Support for Cavium 100Gbps+ OCTEON III Multicore MIPS64 Processor Family

Macraigor Systems announced support for the new state-of-the art OCTEON® III MIPS64 family of 1 - 48 core multicore processors from Cavium. Macraigor Systems' hardware and software solutions are used in a broad range of markets for the development of embedded systems.

As a Cavium PACE (Partnership to Accelerate Customer End-solutions) member, Macraigor Systems offers JTAG-based solutions for all of the steps involved with product development. Low level debuggers and boundary-scan tools are available to help with basic board bring-up all the way through the Eclipse Environment with the appropriate plug-ins to enable application development. Flash memory programming and production line test tools are also offered, all supporting the OCTEON III.

"Deciding to support the OCTEON III was a simple decision. We support the other OCTEON families and have a close working relationship with Cavium and many of their customers," said Craig Haller, Managing Partner of Macraigor Systems.

"With Macraigor Systems' expanded support for OCTEON III, our joint customers will continue to get access to flexible, easy-to-use hardware and software debug tools," said Tasha Castañeda, Senior Strategic Alliance Manager at Cavium. "Macraigor Systems has a strong track record of supplying outstanding solutions and support that has helped multiple OEMs speed their OCTEON-based systems to market."

The recently announced Cavium OCTEON III family delivers breakthrough performance and application-aware features for enterprise, data center, and access and service provider applications. Cavium OCTEON III processors are optimized for use in cloud computing, high-end core and edge routers, metro Ethernet, enterprise switches, 3G/4G/LTE base-stations, enterprise security gateways and appliances, storage networking and mobile core infrastructure equipment.

The OCTEON III family integrates 1 to 48 MIPS64 cores, at up to 2.5GHz, providing up to 120GHz of industry-leading 64 bit compute power per chip. Multiple chips can be combined into a single logical high-performance processor using Cavium's innovative new chip interconnect architecture. All OCTEON III processors also incorporate new dedicated hardware engines to speed search, protocol parsing and traffic management as well as enhanced cryptography, compression and deep packet inspection engines.

For more information about OCTEON III please visit:
http://www.caviumnetworks.com/OCTEON-III_CN7XXX.html [1].

Posted by Janine E. Mooney, Editor

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[1] http://www.caviumnetworks.com/OCTEON-III_CN7XXX.html