Multichannel Data Converter More Than Doubles Signal Bandwidth

Pentek announced its fastest ever multichannel data converter with digital down and up converters. With two channels each of 12-bit, 500 MHz A/D and 16-bit, 800 MHz D/A, the Model 71651 delivers more than twice the bandwidth of Pentek's previous data converters. As a member of the popular Cobalt™ family of high-performance XMC modules, the Model 71651 has a Xilinx Virtex-6 FPGA at its core. The FPGA is preconfigured with data acquisition and playback IP to give the module turn-key functionality, with room left for user customization.

"The Model 71651 handles a tremendous breadth of communications and radar

signals," commented Rodger Hosking, vice president of Pentek. "With its high speed data converters and digital up/down converters, tuning bandwidths range from 10 kHz to 240 MHz, two and a half times our previous modules." Hosking also pointed out that the 71651 FPGA is preconfigured for use out of the box. "Our embedded IP was inspired by what our customers most often require for their applications. We're simply giving them a quick start towards their final configuration."

The Model 71651 features two input and two output RF channels, transformer-coupled to allow direct connection to HF or IF radio stages. The input channels feature 12-bit, 500 MHz A/Ds that feed data into the Virtex-6 FPGA. The output channels incorporate a Texas Instruments DAC5688 digital upconverter that translates real or complex baseband signals to any IF frequency up to 380 MHz. Dual 16-bit, 800 MHz D/As create real or in-phase (I) and quadrature (Q) analog outputs.

Built-in Acquisition and Playback IP

Four types of pre-configured IP in the FPGA help simplify the capture, movement, and playback of data. Three Acquisition IP modules accept data from any of the A/Ds, a test signal generator, or the Playback IP in loopback mode. These acquisition modules each have a private memory bank for storing data in capture mode, or to serve as a FIFO buffer for the linked-list DMA engine to move data off-board through the x8 Gen 2 PCIe interface. The DMA engines can automatically generate meta-data to simplify host processing.

Each Acquisition Module includes a powerful DDC IP core with flexible input selection. Each DDC has an independent 32-bit tuning frequency from 0 Hz to the A/D sampling frequency, and an independent decimation setting from 2 to 131,072. The decimation filters accept user-supplied coefficients and deliver complex (I and Q) output data streams.

In addition to the DDCs, the 71651 features a complete beamforming subsystem. Each DDC core contains programmable I and Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output and performs threshold detection. A programmable summation block handles any of the three DDC core outputs, automatically compensating for summation bit growth. For larger systems, multiple 71651 modules can be chained together via a built-in Xilinx Aurora 4X gigabit serial interface.

The D/A Waveform Playback Module provides a linked-list controller so users can easily deliver waveforms stored in on-board or host memory to the D/As. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. Parameters for each waveform include length of waveform, delay from playback trigger, waveform repetition, plus the link to the next waveform.

Development Tools

Users can also implement their own IP in the 71651's FPGA using Pentek's GateFlow FPGA design kit. Boards can be populated with a variety of FPGAs to match the specific requirement of the processing task.

Pentek's ReadyFlow Board Support package for Windows, Linux or VxWorks operating systems includes C-callable libraries, drivers, and example code for easy access to all of the features. The Signal Analyzer features a virtual oscilloscope and spectrum analyzer for viewing live data streaming from the 71651, straight out of the box. A command line interpreter allows customers to change module parameters to check operation and performance on the Signal Analyzer without having to compile C code.

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