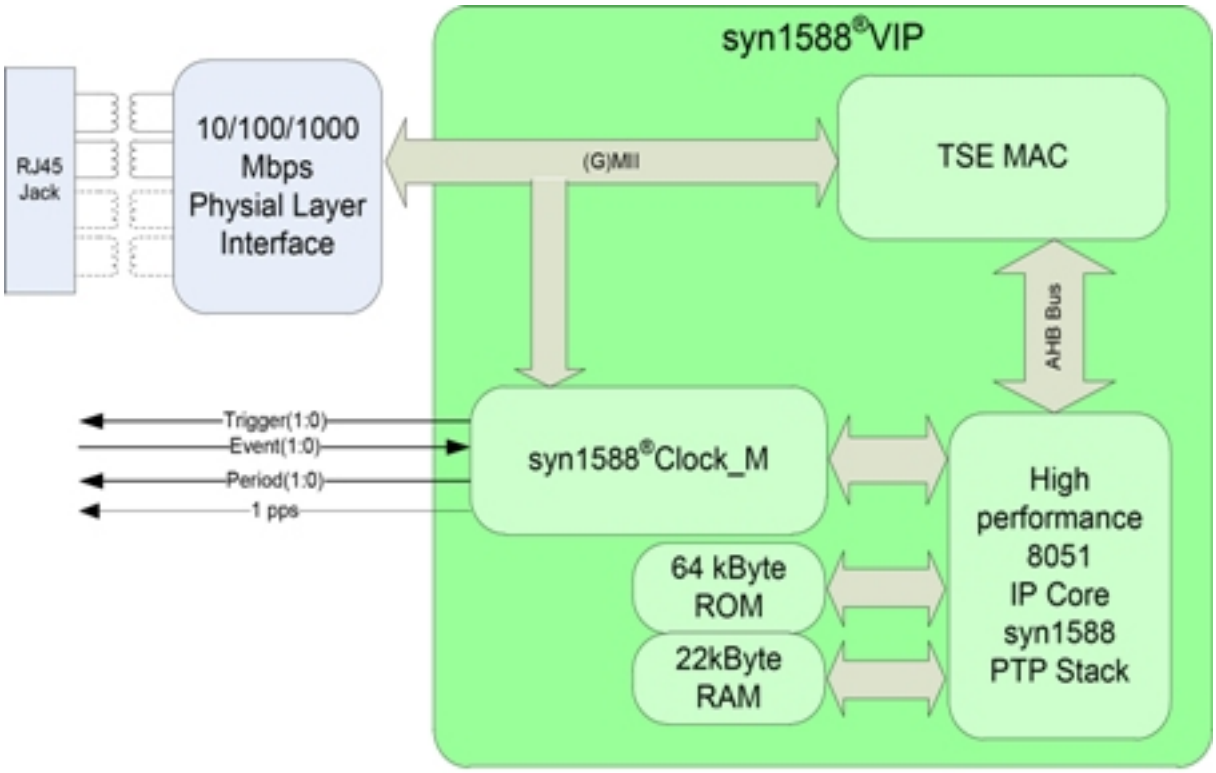
Lattice and Oregano Systems Announce Comprehensive Versions of the IEEE-1588 Timing Node System IP Core



syn1588® Versatile IP - Fully Integrated Network Clock Synchronization Solution

Lattice Semiconductor Corporation and Oregano Systems - Design & Consulting announced the immediate availability of three comprehensive versions of the IEEE-1588 Timing Node System IP core for the LatticeECP3 and LatticeECP2M FPGA families. These SoC-class versions of the IP core are characterized by different levels of functionality and performance.

“We are pleased to strengthen our long-standing relationship with Lattice Semiconductor. The breadth and depth of this solution has grown from just the hardware component of the IP to complete and robust SoC-class solutions for use with the LatticeECP3 and LatticeECP2M FPGA families,” said Nikolas Kerö, CEO of Oregano Systems. “Our quality syn1588 System IP cores have been thoroughly tested to ensure compliance with any associated standard.”

The deterministic and lossless delivery of packets over a network has become a major requirement in Carrier Ethernet, Data Center Ethernet and Industrial Ethernet applications, requiring precise synchronization. The baseline implementation is a single instance of the System IP core that contains a complete hardware and software implementation. The hardware is capable of handling arbitrary clock frequencies while allowing for robust clock state and rate synchronization. Both

analog and digital PLL control loops are supported. Additionally, a highly optimized embedded implementation of the 8051 microcontroller enables an extremely small footprint implementation of the Precision Timing Protocol. Furthermore, this System IP core supports remote configuration and management via IEEE-1588 Management Messages, including in-field upgrades that enable the customer to use it either as a stand-alone SoC implementation or as a System IP Core along with the customer's mission logic. An extensive test bench can be provided by Oregano upon request.

A DUAL instance version of the System IP core is also available. In this version, one instance acts as a PTP master and the other as a PTP slave with different profiles. A multi-core implementation of the 8-bit microcontroller is supported by sharing the program ROM, and only one external oscillator is required for both ports, reducing the total solution cost. If a higher message rate, up to 10K messages per second, is required then the DUAL HP (high performance) version of the IP core addresses this requirement. The SYNC message generation for every client has been moved from software into hardware, reducing the 8051 microcontroller load to just the configuration and control of the packet engine.

"Our goal in working with Oregano Systems is to provide access to world class, comprehensive solutions that enable our customers to use them either as an ASSP or to jumpstart their FPGA-based development," said Lalit Merani, Senior Manager of Product Marketing at Lattice Semiconductor. "The multiple versions of the System IP core provide our customers even more flexibility to choose the right cost and performance point for their specific application requirements."

About the Lattice ECP3 FPGA Family
The LatticeECP3 FPGA family is comprised of the lowest power, SERDES-enabled FPGAs in the market today. The family's five FPGAs offer standards-compliant, multi-protocol 3.2G SERDES, DDR1/2/3 memory interfaces and high performance, cascadable DSP slices that are ideal for RF, baseband and image signal processing. Toggling at 1Gbps, the LatticeECP3 FPGAs also feature fast LVDS I/O as well as embedded memory of up to 6.8 Mbits. Logic density varies from 17K LUTs to 149K LUTs with up to 586 user I/O. The LatticeECP3 FPGA family is ideally suited for deployment in high volume cost- and power-sensitive video camera and display, wireline and wireless infrastructure applications.

For more information, visit www.latticesemi.com [1].

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[1] http://www.latticesemi.com