High Channel Count Software Radio Module Targets Toughest Radar, UAV and Communication Apps

Pentek, Inc. today announced its latest addition to the popular CobaltÂ® family of Xilinx Virtex-6 FPGA boards, the Model 71662 four channel, 200 MHz, 16-bit data acquisition board with built-in digital down converters (DDCs). With an input bandwidth from 300 kHz to 700 MHz, the board is suitable for direct connection to IF or RF ports of communications, unmanned autonomous vehicle (UAV) and radar systems for real-time DSP tasks such as demodulation and decoding. Together with Pentekâ€™s ReadyFlow board support package, with its built-in command line interface and signal viewer, the Model 71662 forms a complete solution for data acquisition, processing and analysis.

The 71662 provides four transformer-isolated input channels that each supply a Texas Instruments ADS5485 16-bit, 200 MHz ADC. The ADC outputs pass to an input multiplexer that supports four Acquisition IP modules factory-installed in the Xilinx Virtex-6 FPGA. Each IP module can receive data from any of the four ADCs, or from a test signal generator, providing highly flexible input and antenna assignments.

Four 512 MB DDR3 SDRAM memory banks, one for each IP module, can buffer data in a FIFO mode or store data in a transient capture mode. All memory banks have DMA engines for streaming data at up to 1600 MB/second through the PCIe interface to off-board storage or additional processing. These linked-list engines offer a unique acquisition Gate Driven mode in which the gate duration determines the transfer length, eliminating the need for pre-set transfer lengths. To simplify post-acquisition analysis of multi-channel data, the DMA engines can automatically construct meta-data packets that contain information such as channel ID, a sample-accurate time stamp and data length.

Also contained within each of the four Acquisition IP modules is an 8-channel digital downconverter bank. Each DDC bank has its own decimation setting from 16 to 8192, providing a wide range of independent output signal bandwidths. The decimation FIR filter within each bank accepts a unique set of 18-bit user-supplied coefficients for custom channel shaping. Each of the eight DDC channels within a bank can have its own 32-bit tuning-frequency setting and delivers a complex output stream consisting of 24-bit I and 24-bit Q samples.

The installed Acquisition IP modules in the 71662â€™s on-board Virtex-6 FPGA allows users to implement their own logic designs. A variety of FPGA sizes are available for the 71662 so that users can obtain as much, or as little, capacity as they need. The SXT devices, for instance, offer up to 2016 DSP slices for applications such as real-time signal demodulation, decoding and forwarding by an UAV monitoring communications in hostile areas. For applications with less-demanding requirements, the lower-cost LXT series is available.

To support custom design in the 71662, Pentek offers the ReadyFlow board support package and the GateFlow FPGA Design Kit. ReadyFlow provides features such as turnkey signal analysis software and a command line interface for controlling the moduleâ€™s operation in an application program. GateFlow includes all of the board's factory-installed IP as documented source code, as well as a library of other functions so that developers can integrate their own IP with Pentekâ€™s. All data and control paths are accessible within the FPGA.

The Model 71662 XMC pricing starts at $12,750 USD with delivery of 8-10 weeks ARO.

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