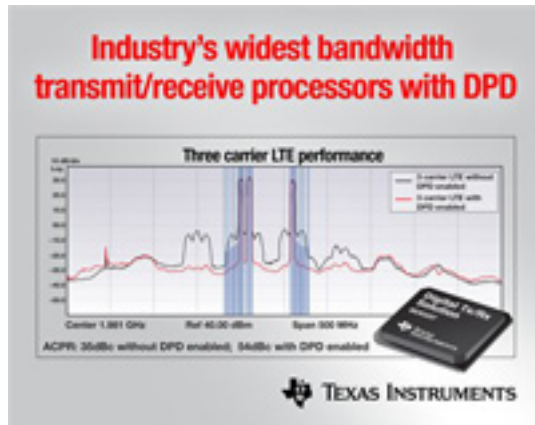


Processors Provide up to 148 MHz of Corrected Transmit Bandwidth with Complete Digital Up, Down Convert Chains



DALLAS, /PRNewswire/ -- Texas Instruments

Incorporated (TI) introduced the industry's widest bandwidth, fully-integrated transmit/receive processors with digital pre-distortion (DPD) for 3G and 4G wireless base stations, remote radio heads and government communication systems.

The GC533x family features two turn-key processors that provide a complete and highly flexible digital transmit and receive solution for wide-bandwidth and multi-antenna wireless base stations at a fraction of the cost of high-gate-count FPGAs and without the time and investment required to develop a custom ASIC solution. A complete system evaluation and reference design kit, which TI will showcase at Mobile World Congress (Hall 8, Stand 8A84), is also available. For more information and to order samples of the GC533x family, visit www.ti.com/gc533x-pr.

The GC533x family provides up to 148 MHz of fifth order corrected transmit bandwidth with crest factor reduction (CFR), along with wideband digital up/down converters with fractional re-samplers, 48-bit numerically controlled oscillators (NCO) and automatic gain control that can support four transmit and eight receive antennas simultaneously.

When combined with the low-cost, high-performance TMS320C6748 floating point DSP, the GC533x platform offers customers a high-performance adaptive DPD algorithm or the ability to implement their own DPD IP.

Key features and benefits include:

- * Provides up to 148 MHz of fifth order corrected DPD bandwidth across two transmitters with CFR 2 dB better than competitive solutions, enabling power amplifier efficiencies as high as 40 percent in three carrier LTE operation with 54-dB adjacent channel leakage ratio (ACLR) and 48-dBm output.

- * Delivers 20 dB of ACLR improvement compared to uncorrected signals in wide-

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bandwidth applications and 40 dB improvement in narrow-bandwidth applications while offering multi-channel, multi-carrier, multi-mode and multi-band support for standards such as 3GPP, MC-GSM, WiMAX, WiBRO and 3GPP2.

* Includes interfaces for up to four transmit and eight receive antennas and a real or complex observation path, enabling 2x2, 2x4, 4x4 and 4x8 transmit/receive solutions while simplifying board layout and reducing cost by an order of magnitude compared to FPGAs.

* Features 48 digital up/down convert channels configurable for data rates as wide as 184 MS/s with four fractional re-samplers, 48-bit NCOs and a bulk up-converter that enables expanded clocking and frequency planning flexibility.

* Integrates I/Q imbalance correction for enhanced performance of wideband complex receive and DPD observation signal chains, enabling lower sample rate and lower-cost receive and feedback analog-to-digital converters (ADCs).

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