Cadence Accelerates SoC Realization, Reduces Costs With New Open Integration Platform

Cadence Design Systems, Inc. today announced the Cadence Open Integration Platform, a platform that significantly reduces SoC development costs, improves quality and accelerates production schedules. A key pillar in support of its EDA360 vision for next-generation application-driven development, the Cadence Open Integration Platform comprises integration-optimized IP from the company and its ecosystem participants; the new Cadence Integration Design Environment; and on-demand integration services.

Cadence mixed-signal (analog and digital) design, verification and implementation products and solutions are the underpinning of the Open Integration Platform. "At GLOBALFOUNDRIES, we are focused on providing time-to-volume leadership on advanced technologies to our customers," said Walter Ng, vice president of the IP ecosystem at GLOBALFOUNDRIES. "Collaboration in delivering application-optimized platforms to our customers is essential to sustaining this leadership. We welcome the Cadence Open Integration Platform's collaborative approach, as this will offer greater choice across the design ecosystem."

Development costs for the creation, qualification, acquisition and integration of IP into system-on-chip (SoC) designs are skyrocketing - in some cases accounting for as much as 25 percent of the total hardware design spend. The Cadence Open Integration Platform helps to reduce those costs by concentrating on an application-driven development process, and encouraging open, standards-based collaboration within an ecosystem of production-proven semiconductor design companies, IP providers, foundries, service providers, EDA vendors and assembly houses.

The ecosystem participants providing the foundational IP to the Open Integration Platform at launch include Cadence, GDA (a subsidiary of L&T Infotech), IBM, RapidBridge and Sonics. As this ecosystem grows, development teams adopting an application-driven approach to design will have a rich portfolio from which to choose silicon-proven IP for standards-based I/O, memory and fabric, along with integration-optimized IP stacks and subsystems.

The new Cadence Integration Design Environment is a comprehensive suite of products that enable developers to create, evaluate, acquire and integrate IP into a SoC -- optimizing from the physical layer through the controller and up to the bare metal software. It is based on existing technologies that include Cadence Chip Planning Solutions, Incisive Enterprise Manager and low-power and mixed-signal solutions.

"For every dollar spent on IP, significantly more is spent on qualifying, acquiring and integrating that IP into the device design," said Nimish Modi, senior vice president, research and development, at Cadence. "The Cadence Open Integration

Platform enables design teams to deliver higher quality, optimized SoCs with lower realization costs. Additionally, this enables designers to focus on differentiation through value-added content rather than spending significant resources and effort on activities that are better handled through packaged offerings or automation."

Development teams can begin using the Cadence Open Integration Platform immediately. Cadence support teams will work with designers to identify the appropriate integrated IP offerings and provide the integrated support services needed to begin approaching development from an application-centric approach. The Integration Design Environment will be available from Cadence in Q4 2010.

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