SPI4.2 Cores Provide Enhanced Buffer Management Features

Lattice Semiconductor Corporation announces that its LatticeSCM FPGA family-based SPI4.2 MACO (Masked Array for Cost Optimization) cores have been enhanced by adding link layer buffer management options. These features provide the option to use a parameterizable buffer manager for applications needing per-channel bandwidth management. The platform provides multiple hardened SPI4.2 cores, using proprietary MACO structured ASIC technology that delivers pre-engineered, standard-compliant IP functions that shorten end-system time to market, lowering device cost, power and PCB footprint targets. Integrated into the LatticeSC devices are high-channel count SERDES blocks supporting 3.8-Gbps data rates, PURESPEED parallel I/O, providing 2-Gbps speed, clock management structures, FPGA logic operating at 500 MHz and large amounts of block RAM.