Σ Δ A/D Converters Fill the Gap

A low noise, wide bandwidth family of continuous-time sigma-delta (CTSD) analog-to-digital converters (ADCs) is available from Analog Devices. The 16-bit, AD9261 and AD9262 CTSD converter, and the AD9267 CTSD modulator couple low noise and high dynamic range with a bandwidth of up to 10 MHz. The AD9267 is exportable to China.

The ADC family achieves its unique combination of speed, accuracy and bandwidth by incorporating a breakthrough CTSD converter technology that is suited for wireless infrastructure, medical and other high-performance equipment demanding uncompromised data resolution and wide bandwidth.

The highly integrated CTSD architecture eliminates multiple discrete components at the system level, while simultaneously improving performance and simplifying product development.

Pipeline and SAR ADC architectures are common analog architectures today. Pipeline ADCs are typically used for wireless infrastructure, video processing and other applications where performance requirements dictate wide bandwidth. SAR ADCs are usually used for industrial controls and data acquisition systems where precision and low-noise are key performance factors. Until now, a performance gap existed between pipeline and SAR ADCs because there were no converters that could meet the conversion needs of emerging technologies that simultaneously demand high dynamic range, wide bandwidth and low power. The AD926x CTSD ADCs fill this performance gap by efficiently delivering wide bandwidth and greater accuracy while significantly reducing system level complexity.

The AD926x utilizes principles of over sampling, noise shaping and input characteristics unique to its architecture to achieve high levels of performance and ease of use. The quiet resistive input structure relaxes the requirements of the driver amplifier while the higher order over-sampled continuous time loop filter attenuates out-of-band signals reducing the need for large baseband filters and other signal conditioning circuitry. The high dynamic range performance reduces or eliminates the need for automatic gain control in many applications. These features coupled with a wide input bandwidth simplify system design, reducing the overall system footprint and shortening time-to-market. By offering design engineers a choice of ADC architectures, ADI can support any signal chain regardless of whether performance requirements demand high speed, precision, low power or any combination of the three.

The 16-bit single and dual AD926x ADC family achieves excellent performance with a combination of 86 dB dynamic range for an input signal bandwidth of up to 10 MHz. The highly integrated AD9261 and AD9262 feature an on-chip PLL clock multiplier, decimation filters, and sample rate converters and provide flexible output data rates between 30 MSPS and 160 MSPS. The AD9267, which features

only the high performance 640 MSPS modulator core and PLL clock multiplier, presents the high speed data directly to the output. This provides designers the flexibility to offload signal processing functions to an FPGA or other processor. The 150 mW per channel to 350 mW per channel power consumption of the CTSD converters is matched to a range of communications and industrial applications, including emerging radio architectures, such as direct down conversion, where the dual AD9262 and AD9267 can be used to support multiple wireless carriers and standards simultaneously.

The AD926x CTSD ADC family is sampling now and will be available in volume production in April 2009.

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