How FPGA Trends Impact Wireless Infrastructure Design Organizations

While many skills are necessary to develop FPGA designs, a team-based design methodology approach proves to be both effective and efficient.

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With the introduction of 40 nm field programmable gate arrays (FPGAs), the design domains of wireless infrastructure electronics that can be addressed with programmable logic devices (PLDs) are growing (see Figure 1). This is a response to ever-changing wireless requirements, as well as a function of the rising cost of new ASIC starts in successive generations of silicon geometry. Functions that were once restricted to ASIC designs or DSP processor-based systems now benefit from the shorter design cycle times and simpler hardware verification processes of an FPGA.

Though this leads to important efficiencies in wireless infrastructure systems design, it also has a fundamental effect on the systems engineering process, as well as the management of engineering organizations in these types of wireless programs. By examining several ways that FPGAs are expanding system design roles, there are several conclusions that can be drawn that impact the mix of talent needed in engineering organizations, as well as their organizational structure.?

Wireless User Requirements

The user requirements for wireless infrastructure equipment are becoming increasingly complex as well as sensitive to time-to-market pressures for OEMs.

One particular application example is the digital RF/IF card or the remote radio head shown in Figure 1. New, larger programmable logic devices offer an ideal solution to integrate flexible, scalable, and reprogrammable circuitry for multi-standard, multi-mode digital RF/IF SoC in a productive design flow that allows for simple technical upgrades without reinventing critical IP. In fact, this is a requirement driven by the mobile operators on the OEMs.

The other technical requirements are the need for flexibility by offering multi-standard multi-mode capability. Some of the BTS OEMs intend on supporting MC-GSM, LTE and WCDMA on the same frequency bands as in inlay or overlay. LTE, WiMAX and HSPA+ will support MIMO configurations as well. This means that more channels need to be supported. All these technical requirements are driving the need for significantly higher integration. These are the initiatives in wireless infrastructure technology that are being addressed by the larger class of new FPGA devices.

Engineering Organizational Structure

Historically, engineering organizations have been designed around one of two large classes: functional organizations and project organizations (see Figure 2). Most engineers and managers are familiar with the differences between these two classes. Functional organizations are built around engineering or sub-product engineering proficiencies, allowing for a focus on technology and engineering best practices. Project organizations are built around a specific customer product so that engineering talent is focused on the specific needs of a customer. Both classes have their situational advantages and disadvantages.

With a larger portion of a system encapsulated in FPGA logic, there are two effects on functional engineering organizations. The first, predictably, is a higher demand for FPGA design engineers on staff, and possibly realignment in the engineering subdivisions. The second impact is to pull systems and architectural engineers into the FPGA design effort. This requires either a strong systems engineering capability within the hardware and firmware organization or a systems engineering staff capable of understanding the complex and new capabilities of programmable logic devices.

Project organizations are better suited for large re-engineering programs to take advantage of new 40 nm technologies; however they are less likely to be tracking advances in digital technology. Functional organizations are more likely to be technology focused and able to translate new technologies across multiple programs. ?However, the momentum to adopt new chip technologies is sometimes lacking compared to that of a project organization. In both cases, some fundamental changes may be necessary in the systems engineering functions to take advantage of design efficiency advantages for design integration into larger FPGA devices.

System Design Approach Changes

The systems engineering process is impacted when several subsystems are consolidated into larger FPGA devices and then distributed among responsible engineers. Fundamentally, the principles of requirements engineering and test do not change. However, the lines between hardware and software can become more difficult, and the concept of design interfaces expands to include data boundaries between FPGA sections (within the FPGA), a trend that has existed in software engineering for some time.

Just as systems engineering now includes code and mega-executable partitioning among software team members, it also now encompasses FPGA architecture and design. When using larger FPGA devices, FPGA component selection is being driven much more by system requirements than hardware requirements.

FPGA Design: What Skills are Needed?

One of the most difficult skill sets to gain in design organizations today is ‘FPGA design’, where the job descriptions include:

• Strong VHDL and Verilog design experience?• Embedded computing experience?•

Digital test and debug (logic analyzer) experience?• DMA and memory interface experience?• DSP experience with FIR filters, multi-stage decimation, interpolation, DUC, DDC, NCO, CFR, and DPD techniques?• Familiarity with CPRI or OBSAI RP3, RP3-01 interfaces?• Familiarity with FFT and OFDMA?• An ability to make systems engineering trade-offs between cost and performance focusing on business concepts.?

Many of these skills are necessary to develop FPGA designs, but these skills can now be distributed among a team rather than consolidated into a small number of FPGA-knowledgeable design staff. As in software engineering, new skills are needed in FPGA architecture and design partitioning. These are systems engineering functions and should require only a subset of FPGA design engineering skills.

Designing the New 'Electronics ?Engineering' Organization

Moving up the silicon manufacturing technology curve may not seem like a good reason for reorganization. However, the reason to move to larger devices should be based on integration efficiencies and design productivity, which may necessitate changes in design roles.

Redefining Systems Engineering

The systems engineering roles in companies are evolving in many ways. Among the changes in scope are the inclusion of life cycle management, design-for-cost and manufacturability, system of systems design, and open standards architectures (to include IP reuse). These are all derivatives of a 'team-based design' methodology aimed at generating efficiencies elsewhere in the design lifecycle.

Cost drivers in wireless infrastructure design – architecture, partitioning, verification, and board integration – are more strongly tied to design tool flow than ever before. With the potential for different vendors in each portion of the design flow, there is a great deal of risk to be managed by the engineering organization.?

The fundamental structure of an organization should enable it to manage tool flow risk, as well as the IP reuse throughout the organization. While there are many possible ways to tailor this to wireless infrastructure company organizations, advocating a 'team-based design' function controlled by a systems group or IP management staff is the most effective and efficient.

The example in Figure 3, team-based design and tool flow are emphasized placing all IPT managers within that organization. The primary function of the IPT lead is to pursue a systems design using the best possible architecture given the current technology in tools and team-based design. ?

Design flow methodology is a critical technology and a cost driver for organizations that rely on PLD design, talent and project management potentials should be driven towards these competencies as (one) path for career advancement.

Time to Focus on Design Flow

While there are many temptations to focus on the newest high density and high speed transceiver capabilities of the 40 nm generation of FPGA devices, wireless customers will necessarily want to focus their efforts on the impact of design flow technology in their organizations (see Figure 4.)

Trade studies for device selection are traditionally cost versus performance. As FPGAs become more capable of containing enough of an electronic system's functions, the number one systems cost driver is tool flow efficiency. While this is not simple to assess or measure, selecting the right tool flow for wireless electronics design is paramount for cost competitiveness and efficient organizational operation.??WDD?
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