130 nm SiGe BiCMOS Processes Optimize Cost and Performance

HBTs feature a uniquely engineered fabrication process and new epitaxial materials optimized for wireless communications systems.

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Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) are capable of much better performance than comparably sized CMOS devices. This technology

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advantage is critical for wireless applications designed in SiGe BiCMOS that require integration of high performance analog blocks such as a low noise front end or power amplifiers in a System-on-Chip (SoC) solution. The addition of the SiGe HBT provides the low power RF building blocks that are not available in advanced CMOS and complements the advanced digital integration of the SoC.

Foundries offering specialty technologies such as SiGe have put significant effort toward developing low cost alternatives to 130- and 90 nm CMOS to allow designers to make a decision on process technology by giving equal weight to both cost and performance benefits. Low cost SiGe HBTs are introduced into a 130 nm CMOS baseline process, reducing the bipolar complexity by over 50% to create a technology that outperforms its CMOS peers at the same price point. This approach provides IC designers with the flexibility to optimize both cost and performance of wireless systems at the 130 nm technology node.

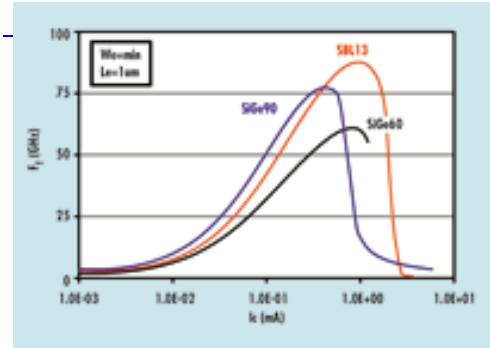
Like CMOS, SiGe BiCMOS technology continues to follow Moore’s Law and is now in production at the 130 nm node. One of the advantages of the BiCMOS platform has always been the extremely high performance of the bipolar HBT devices, which generally exceed the performance of CMOS FETs. This has allowed higher speed and higher performance analog/RF/mixed-signal ICs to be designed in larger geometry SiGe BiCMOS and achieve results not attainable in CMOS.

Speed however, is not always the most important technology feature. Cost and

integration are key to next generation technologies. SiGe BiCMOS technology plays an important role in the development of high speed, low-cost products in several different markets with mixed-signal IC components. Because SiGe BiCMOS is based on a Si CMOS platform and incorporates high speed HBTs, it is ideally suited for high volume applications where CMOS cannot provide the necessary performance and more exotic materials are too expensive. This also adds design flexibility by facilitating system partitioning of a SoC into separate blocks of analog and digital content. Given that 130 nm SiGe BiCMOS is now available, a wide range of products can be designed on a ubiquitous technology node with increased performance and low cost. Wireless systems require the low power, low supply voltages and greater digital density available at the 130 nm node. The key for foundries is to optimize the technology performance with a cost model that these applications require. High performance 130 nm SiGe HBTs are capable of switching at speeds in excess of 300 GHz, but at a cost that prohibits any large market adoption. A new 130 nm SiGe BiCMOS technology platform that combines the performance of high speed, low voltage CMOS with a hybrid, low cost SiGe HBT addresses both the cost and performance requirements of the wireless and tuner markets.

Low-Cost SiGe BiCMOS

The high performance of the SiGe HBT results from the use of advanced materials and process techniques which typically increases the technology cost. However, new HBTs have been developed



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with a uniquely engineered fabrication process and new epitaxial materials optimized for wireless communications systems. These new low cost SiGe HBTs are suitable for advanced wireless communication ICs because of improved performance compared to 60 GHz technology and cost savings compared to 150 GHz technology. Combining these SiGe HBT devices with 130 nm CMOS provides the designer with a new tool in low cost circuit designs.

These HBTs have been developed by optimizing the standard fabrication process on the 130 nm node as shown in Figure 1. Key to this optimization is the combination of several process steps and masking layers as well as improvements made in the emitter formation and collector design. High speed devices usually employ a self-aligned emitter and collector epitaxial material to achieve their performance. These devices trade off high speed for lower device complexity using only a quasi self-aligned emitter, no collector epi material, and implants shared with the CMOS device formation. This produces a more robust, higher yielding process

with sufficient speed for wireless applications.

The reduced complexity HBT has electrical performance that provides peak Ft of 90 GHz, which is sufficient for most commercial wireless applications that operate at 1 to 5 GHz, while retaining the low noise and higher power handling advantage of the bipolar device. Figure 2 shows the performance of the SiGe HBT (SBL13) compared with production 60 and 90 GHz HBT (SiGe60 and SiGe90) technologies for a minimum emitter width and 1 &#181m emitter length. The cost/performance trade-off is optimized in this BiCMOS process such that there is no premium paid for additional speed that is not needed.

Even with a 90 GHz SiGe HBT available in the process, the cost savings can be significant. The SiGe HBT module allows die costs to be reduced by up to 40% compared to a high performance 120 GHz BiCMOS technology because of fewer fabrication steps. As CMOS geometries approach 65 nm, digital circuits become denser, but analog performance becomes more complicated due to scaling limitations and complex DFM rules. 130 nm SiGe BiCMOS technology provides an ideal node to integrate mixed-signal circuits providing both high performance analog CMOS and SiGe HBTs. By using the low cost 130 nm SiGe BiCMOS technology, there is a reduction in analog/RF die size, and therefore die cost, by 25% compared to 130 nm CMOS and 37% compared to 90 nm CMOS. In Figure 3, the cost benefits of SiGe BiCMOS are clearly evident for high speed applications (where Ft &gt125 GHz is needed), while low cost CMOS dominates when performance is not an issue. This new low-cost technology approach makes the 130 nm SiGe BiCMOS a cost competitive node that is well suited for wireless applications.

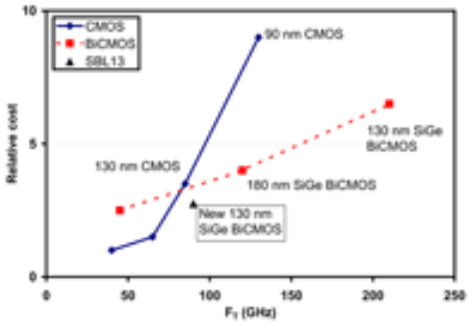
Further cost savings can be realized by eliminating the expensive Cu back-end metal processes. Advanced digital processes require Cu metallization and low-k dielectric materials in order to maintain high-density digital circuitry. Analog applications can realize the cost savings associated with Al metallization and relaxed back-end lithography processes while maintaining interconnect and inductor performance. Using a 150 nm Al interconnect instead of a 130 nm Cu interconnect can provide up to 30% cost savings in an analog design without compromising die size or performance due to the digital blocks.

Photomask costs are also a significant component to the costs of product development. The reduced mask set of the 130 nm SiGe BiCMOS process, due to the advanced process integration, requires only the same number of masking layers as a standard 130 nm CMOS process. With the same number of masks, the BiCMOS mask set cost is comparable to a 130 nm CMOS process and significantly less than a 90 nm CMOS process, but adds the BiCMOS performance and design flexibility.

Wireless System Applications

SiGe BiCMOS has been employed at the 350 and 180 nm nodes extensively in wireless systems because of the design advantages. With the BiCMOS technology flexibility, designers are free to implement better performing circuits with low power and smaller area. Examples include RF transceivers, where SiGe is utilized in the

front end integrated with high density digital blocks, low noise amplifiers, power amplifiers and tuners. These circuits are ideal for



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802.11a/b/g and 802.11n WLAN, Bluetooth, W-CDMA, DVB-H, GPS and other mobile systems. The trend in all of these systems now is to integrate these analog functions into advanced CMOS SoC and live with the performance. The 802.11n WLAN MIMO transceiver is a prime candidate for the 130 nm SiGe BiCMOS technology. Single chip SoC solutions integrate multiple RX and TX blocks along with the MAC and baseband processing circuitry. The 130 nm CMOS provides a die size reduction of up to 25% from a 180 nm node while the SiGe HBT allows the transceiver blocks to meet the high performance requirements while keeping costs low.

In WEDGE transceivers, the CMOS implementation of LNAs and mixers limits circuit performance, and SiGe BiCMOS is ideal for this type of analog intensive IC. Moving to the 130 nm SiGe BiCMOS node allows the designer to port digital IP from other 130 nm designs without extensive redesign and combine it with the low NF and high gain of the low cost HBT. The low NF and Rn of the HBT improve the sensitivity of the receiver circuitry while also meeting the IP3 requirements.

Integrating these circuits in a 130 nm SiGe BiCMOS SoC provides the maximum amount of design IP re-use and leverages the performance both the analog and digital capabilities of this technology.

Conclusion

Advances in foundry fabrication techniques allow for high performance HBTs to be built on mature, high yielding technology nodes without a high price tag. New SiGe BiCMOS processes combine 130 nm CMOS with low cost SiGe HBTs to provide a technology optimized for wireless communications systems. This approach affords IC designers more design bang for the technology buck and is changing the way these systems are developed.

About the Author

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