Introducing a New Approach to Wireless IC Design

As more standards and technologies are packed into chips, traditional design flows are unable to meet the challenges of complex IC architectures.

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Not long ago designers building wireless systems spent much of their time and effort integrating RF, analog and digital components on a system board. The rapid

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evolution of CMOS technology now allows designers to create a wireless system integrating RF, analog and digital filtering and control functions on a single chip. Complicating the design process is the proliferation of a seemingly endless array of wireless standards. Emerging multi-band 3G handsets now often integrate WiLAN, GPS and other technologies into highly dense SiP solutions.

As a result, RF design has become a multidisciplinary task. A growing number of RF, analog and digital functions must now reside, if not on the same chip, at least within the same package. More so than ever, RF, analog and digital designers must work side-by-side to build a solution that meets ambitious performance, cost and time-to-market goals. These same designers must also take verification into account early in the process since it is essential in ensuring time-to-market and first-silicon success.

RF IC designers attempting to accomplish this task face a formidable set of challenges. As ICs grow in complexity and integrate higher levels of analog and mixed-signal content, full chip verification becomes increasingly difficult and time consuming. Cross-domain verification presents a serious challenge that often requires manual intervention. At the same time the massive quantities of data and

long runtimes associated with modeling, parasitic extraction and re-simulation extend product development cycles.

A New Methodology Is Needed

Clearly, traditional microwave or RF component design flows are no longer sufficient to address these many challenges. Designers need a comprehensive simulation strategy and modeling plan to meet their design goals. They need to verify full chip functionality at the transistor level as part of a system-wide functional verification methodology. They also need to perform advanced design exploration analysis to explore parasitic effects and find an optimal solution. IC spiral inductor synthesis and EM verification must be performed early enough in the design cycle to ensure accurate inductor modeling. Additionally, phase lock loop (PLL) design and optimization must be radically simplified.

Most importantly, they need a new methodology that will allow them to apply new EDA technologies and advanced top-down verification strategies to these problems and, in the process, reduce design cycle time and increase silicon predictability without expending large amounts of time learning how to apply these new technologies.

Proven Design Techniques

Figure 1 illustrates a design flow diagram of a new RF design methodology that packages proven design techniques in a system-to-tapeout design kit. This new approach to RF design augments traditional design flows by supplying advanced methodologies optimized for linking systems-level design with IC implementation, managing RLCK parasitics, inductor synthesis and modeling, and introducing functional verification for RF ICs. In the process, it allows RF designers to accurately, but rapidly, verify their complete design across digital, analog and RF domains.

The Kit approach packages proven methodologies and best practices for RF and IC system design along with re-useable, pre-setup components. Detailed step-by-step documentation shows designers how to verify or validate the overall flow. Hands-on workshops help shorten the learning curve.

Within this new approach, designers can validate system conformance of the RF IC using MATLAB/Simulink co-simulations. They can also perform complete spiral inductor synthesis, a

common obstacle to rapid development of wireless ICs, through a comprehensive EM verification flow. Fully extracted RCLK views allow the designer to verify the IC at the top level with information detailed enough to ensure design predictability. The included intelligent RC reduction and simulation strategies can be used to significantly minimize re-simulation runtime. AC noise analysis tools allow the designer to review RF noise distribution patterns and rapidly prototype isolation schemes. To accelerate full chip verification, this new methodology allows designers to develop and validate functional verification models with built-in assertions and perform top-level integration as part of a functional verification test suite.

Still, any new design methodology is only useful if it can be easily and quickly applied to real applications. One of the keys to rapid adoption of this new flow is the demonstration of its capabilities on a segment representative design. Typically this representative design should include block and system level test benches, complete behavioral models, transistor-level schematics, physical layout and parasitic extracted views. In the RF domain, for example, designers using a kit might have access to a complete 802.11 b/g design which includes an RF transceiver with integrated PA, integrated PLL frequency synthesizer and analog baseband. Proven, reusable LNA, down conversion mixers, Rx/Tx band pass filters and power amplifiers can help ensure silicon accuracy.

With this segment representative design, engineers can map these new techniques to their own application. Application consultants can help designers get a jump start on validating the reference design in the customer's design environment by helping setup the environment, customizing the existing methodology and update scripts.

Accelerating PLL Design

One of the more imposing tasks for an RF engineer is designing a PLL. These designs typically feature two widely-spaced time constants and a VCO that often oscillates thousands of times faster than the reference frequency. While FastSPICE simulations allow designers to verify PLL performance at the transistor level, it is extremely difficult to optimize the design using those simulations. Accordingly, designers often don't know when to simulate at the transistor level, when to simulate at the behavioral level and what the implications and benefits are for each strategy.

A PLL simulation guide can help designers address this problem by outlining how to model and characterize a PLL with transistor-level accuracy. The guide can help identify the crucial criteria designers must consider and explain basic design tradeoffs in loop bandwidth and lock time.

Conclusion

Wireless IC design has undergone a radical transformation over the last few years as many more standards and technologies are packed into chips and SiPs. Traditional design flows are no longer able to meet the challenges of increasingly dense and complex IC architectures. Designers clearly need a new approach to RF IC development. By moving to new RF design methodologies that are specifically targeted at the key challenges in the RF domain and demonstrated on a representative design, today's development teams can increase silicon predictability, shorten simulation runtimes, improve productivity and meet today's aggressive time-to-market goals.

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