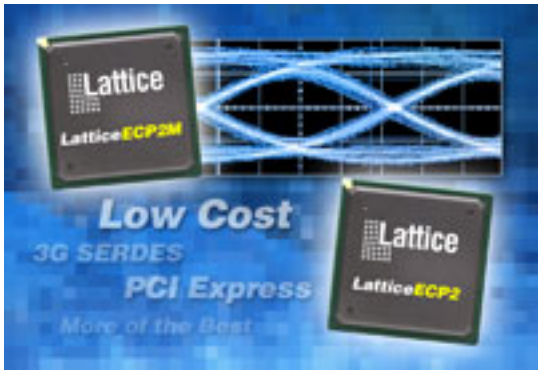
Dynamic Random Access Memory Controller



Lattice Semiconductor Corporation announces the immediate availability of the 533 Mb/s Double Data Rate 2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM) controller Intellectual Property (IP) core supporting a low-cost Field Programmable Gate Array (FPGA) family. This DDR2 SDRAM IP core is optimized for the LatticeECP2 and LatticeECP2M FPGA families, as well as its high-end LatticeSC Extreme Performance FPGA family. The DDR2 SDRAM Controller IP core interfaces seamlessly with industry standard DDR2 SDRAM memory devices and has been performance-tuned for Lattice FPGAs. Not only does this IP core support all DDR2 commands, it also is flexible, with intelligent bank management to minimize active commands, a synchronous implementation for reliable operation and a command pipeline to maximize throughput. The most common memory configurations are supported through a combination of variable address widths for different memory devices, programmable timing parameters, byte level writing through data mask signals and burst termination.

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