Improving Power Amplifier Efficiency in CDMA and WiMAX Systems

Efficient design and implementation of crest factor reduction and PA linearization solutions.

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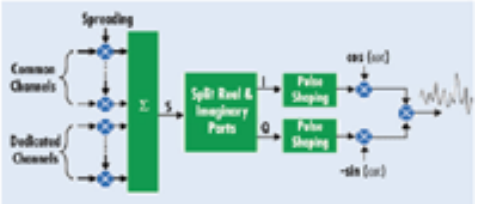
WiMAX is an acronym for Worldwide Interoperability for Microwave Access, a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The WiMAX Forum, formed in 2001, describes WiMAX as “a standards-based technology enabling the delivery of last mile wireless broadband access as an alternative to cable and DSL”.

The orthogonal frequency division multiplexing (OFDM)-based WiMAX 802.16e standard is expected to offer higher data rates compared to the current 3G technologies.



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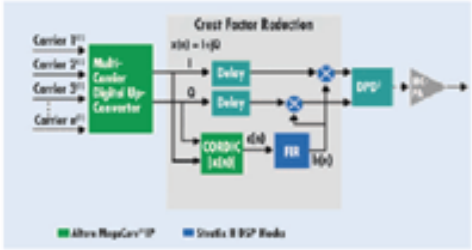
To achieve this goal, the transmitter chain must transmit with high fidelity and power to cover a large area utilizing only a few cell sites. This puts high demand on power amplifier (PA) performance. However, the nature of code-division multiple-access (CDMA) and OFDM signals makes it difficult to achieve high PA efficiency.

As an example, base stations in third generation (3G) CDMA-based systems transmit a composite downlink signal (see Figure 1). This downlink signal is formed by summing up different physical channels. These different physical channels include dedicated data and control channels for different users apart from the always required common control channels.

As the number of users in the system increases, the time-varying composite signal envelope exhibits a high peak-to-average ratio (PAR) or crest factor. Crest factors of the downlink signals are as high as 15 dB for single carrier systems and 20 dB for base stations with multiple CDMA carriers. Similarly, as the number of sub-carriers increases, the PAR of the OFDM signal also increases. Signals with high crest factors degrade the efficiency of the power amplifiers that amplify the downlink signals in base station transmitters.



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The operating point of the PA is reduced or backed off in order to accommodate input signal peaks and to keep waveform distortion within specified limits. Back off is done to maintain linearity at the PA output and prevent out-of-band radiation. Input signals with a high crest factor need large back-off and will lower the efficiency of the PA. Consequently, designers face the challenge of reducing the crest factor of the input signal and preventing the efficiency of the PA from falling to unacceptable levels.

Crest Factor Reduction

Clipping signal peaks is the simplest way of reducing the crest factor. However, hard clipping causes sharp corners in the clipped signal, degrading signal quality and increasing the out-of-band radiation. Peak windowing is a technique that smoothes the sharp corners by multiplying the signal to be clipped with a windowing function and is especially useful for CDMA systems.

The magnitude of the original signal *x(n)* is compared with a threshold value *A* to yield an intermediate scaling factor *c(n)*. This is then convolved with the window coefficients *w(n)* to generate the final windowed scaling factor *b(n)* as shown below:

$$c(n)=\begin{cases} 1 & ,|x(n)|\le A \\ \dfrac{A}{|x(n)|}, & |x(n)|>A \end{cases} \quad \text{and} \quad b(n) = 1-\sum_{k=-\infty}^{\infty}[1-c(k)]w(n-k)$$

A windowing finite impulse response (FIR) filter with a feedback structure can be used to calculate the clipping function *b(n)*. The feedback structure is used to calculate a correction term using the previous input values to prevent over clipping of consecutive samples. Choosing the length of the window L involves a trade-off between the signal quality and the out-of-band radiation. This choice must be selected appropriately to satisfy base station radio transmission requirements.

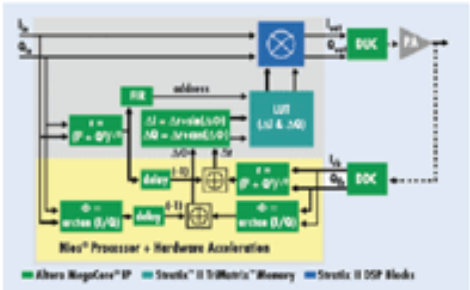
Another CFR technique involves selecting and ordering signals for transmission. The result is a low crest factor. This involves complicated calculations and highly complex hardware at the digital modulation stage. But it can reduce the signal crest

factor without distortion because the CFR system monitors the signal and re-orders the transmission for a low crest factor.

Once the crest factor is reduced, designers are confronted with a signal distortion issue. When signal peaks are smaller, the signal is distorted, which leads to possible violation of the stringent WiMAX -31 db error vector magnitude (EVM) specification. Digital pre-distortion (DPD) remedies this problem. DPD calculates the distortion caused by the PA, defines it, and applies pre-distortion to the input signal. When the signal exits the PA, it is pre-distorted.

Relying on Analog Feed Forward
Designers have generally relied on analog feed-forward (AFF) systems to deal with signal distortion. AFF presents additional design issues. Designers work with analog components requiring fine tuning. Additionally, these components dissipate considerable heat, consume inordinate space and lack the integration possibilities of digital circuits.
AFF is vastly different than DPD. With AFF, a final corrected signal output is generated by finding the difference between the undistorted original input signal and the distorted PA output signal. Therefore, this approach is post-correction, thus the name, feed forward.

Feed forward generates a correction signal, which is applied to the output. The correction signal is derived on-the-fly by subtracting a sample output of the PA from an undistorted



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input sample and amplifying the result in an error amplifier. This system requires no knowledge of the signal and can accept a modulated RF carrier as the only input.

DPD requires the insertion of a non-linear module before the RF power amplifier. This non-linear module, called the pre-distorter, has the inverse response of the PA so that the overall response at the output of the PA is linear. Adaptive DPD involves the digital implementation of the pre-distorter and the presence of a feedback loop that adapts to the changes in the PA response due to varying operating conditions.

Efficient CFR and DPD Hardware Design
Altera provides FPGA-based and DPD reference designs for CDMA systems. The first CFR technique noted earlier requires a FIR filter to implement the peak windowing algorithm. DSP blocks embedded in the FPGA efficiently implement this peak windowing algorithm. Each DSP block operates at over 370 MHz and has a number

of multipliers, followed by adder/subtractor/accumulators in addition to registers for pipelining. The FIR compiler MegaCore is used to calculate window filter coefficients. It also automatically generates code required for the software to synergize high-speed, area-efficient FIR filters of various architectures.

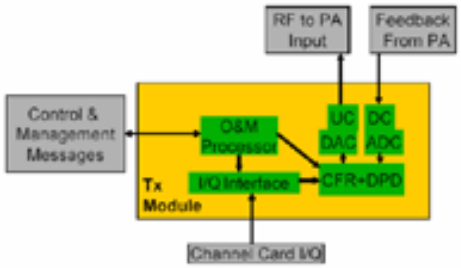
The instantaneous amplitude of the complex symbols are efficiently calculated with a coordinate rotation digital computer (CORDIC) solution. CORDIC is an iterative algorithm that performs various trigonometric functions by using only additions, subtractions and shift operations. CORDIC uses logic elements (LEs) operating in arithmetic mode. Each LE is configured to contain a full adder/subtractor cell plus an associated register. The deeply pipelined, parallel architecture enables operation speeds over 300 MHz.

Figure 3 shows Altera's solution for an adaptive DPD using the blind adaptive LUT-based approach. Incoming samples (I and Q) have correction factors applied from the LUT and sent to the radio frequency (RF) module. The address of the LUT is derived from the input power, and the LUT contains two values for each location, the real part, I, and the imaginary part, Q. In the feedback loop, the output of the PA is downconverted — transformed to polar form — and compared with the delayed version of the input to the pre-distorter in polar form. This error is then used to update the values currently stored in the LUT.

Embedded DSP blocks, RAM and soft core processors play major roles in this effective DPD design. Applying correction factors from the LUT involves complex multiplications that map well into the embedded DSP blocks of the FPGA. Embedded RAM includes 512 bit, 4 kbit, and 512 kbit blocks. The 4 kbit and 512 kbit blocks can be used for LUT implementation, while 512 bit blocks, in shift register mode, are ideal for delaying input samples for error calculation. Thirdly, embedded processors allow designers to quickly modify the DPD adaptive algorithm in software and customize their solution without scheduling complex data paths. This integration of the forward and feedback paths within the FPGA eliminates the need for external DSPs and reduces system costs and board size.

Turn-key WiMAX Radio Head

TelASIC Communications offers a turn-key radio head for WiMAX base stations. The solution consists of a chassis containing the receiver, transmitter with PA linearization, power



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amplifier, operation and maintenance controller, and CPRI-based digital interface to the baseband. TelASIC worked closely with Altera and

used its FPGAs. Figure 4 shows a diagram of TelASIC's WiMAX radio head. It achieves 25 dB linearization correction with 30% power amplifier efficiency and has the ability to support 20 MHz of instantaneous signal bandwidth.

A single FPGA implements TelASIC's WiMAX-specific dynamic CFR (DCFR) and dynamic DPD (DDPD) that linearizes a power amplifier with high efficiency, even at the EVM of 2.5% to transmit up to 40W from a power amplifier using standard off-the-shelf LDMOS transistors. The radio can be configured for one or two carriers (10 MHz each). FPGAs with embedded digital signal processing (DSP) blocks and soft processors provide TelASIC designers with a perfect platform for implementing CFR and pre-distortion solutions. Altera's Nios II embedded processors operate at over 150 MHz and can use custom instructions for hardware acceleration of program code.

TelASIC's linearization technique is "dynamic" because of the high speed of operation and is desirable for quickly tracking changing operating conditions in the power amplifier.
FPGAs were used to develop the DCFR and DDPD designs to reduce the cost of multiple design iterations that, otherwise, would have been incurred in ASIC development. These designs were subsequently migrated from FPGA to Altera's HardCopy structured ASICs as product volumes increased. These structured ASIC-based designs are shipping in volume to lower production costs to ASIC-type levels and to reduce power consumption.

About the Author

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