A New Generation Cartesian Loop Transmitter for Flexible Radio Solutions and Software Defined Radio

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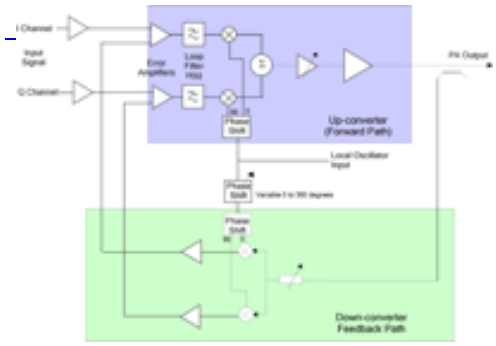
The concept of ‘Software Defined Radio’ (SDR) is much discussed, but in practice can mean many different things to different people and organizations. In essence, the



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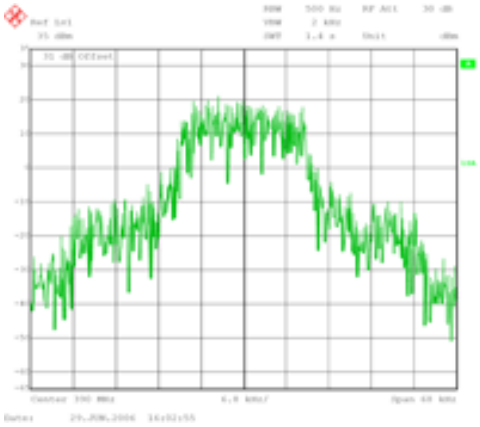
concept is simply the ability of a radio solution to select multiple modes of transmission. More rigorously it might be argued that the same hardware must be used, and software used to generate and demodulate the waveforms. In this context, a great deal of attention is paid to SDR receivers and their ability to deal with differing regulatory requirements, e.g. modulation, bit rate, signal bandwidth, adjacent channel rejection, etc.

Transmitters face similar problems, although varying signal bandwidths are generally less of an issue as long as the digital-to-analog function has suitable performance, but differing modulations and a wide operating frequency can present a greater challenge. A key problem facing the designer occurs if the system must support linear modulations schemes, i.e. modulations which have significant amplitude content. Such modulations present a challenge as either the Power Amplifier (PA) must be inherently very linear, which generally involves very high power consumption; or some form of linearization scheme needs to be used. The challenge then becomes making the linearization scheme work for all the required operating parameters.

The situation is further complicated by another requirement often found in modern radio designs, which is that organizations are frequently looking to maximize the use of a



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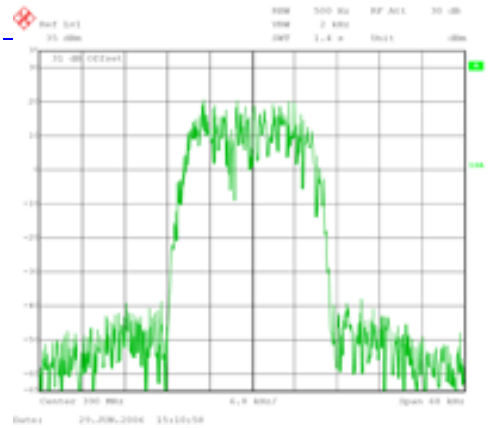
particular solution across a range of designs. This means that one solution often has to meet the requirements of hand portables, mobiles, and, in some cases fixed stations as well. Further, in markets like specialized / professional radio systems or military systems a product can span operating frequencies from, 150 MHz to 1 GHz. This is not necessarily the case in one product, but often build variants must support such a range.

Various linearization schemes come to mind to meet this requirement, but the focus of this article is on Cartesian feedback. It will be seen that with a modern integrated solution this scheme can offer a genuine answer to all the challenges discussed above.

The Cartesian Loop

The Cartesian Feed-back Loop (CFBL), first developed in the 1980's [1,2], is now well established as a solution for highly-efficient linear transmitters using modulation such as ?/4-DQPSK, 8PSK, QAM etc. The scheme has been universally utilized in products implementing the TETRA standard [3], and also widely used in Japanese digital



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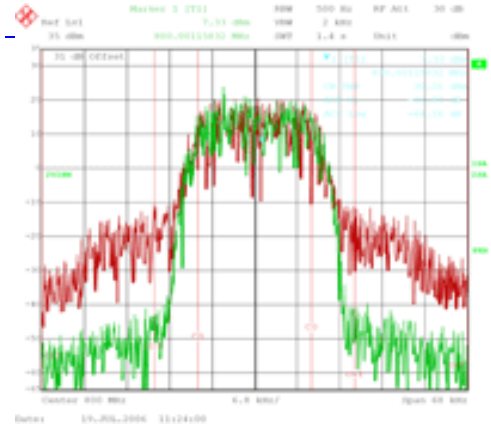
technology. The Cartesian loop has the advantage of offering a large degree of linearization improvement; gains of over 30 dB are not untypical. It is most suited to channel spacing up to about 200 kHz, beyond this, keeping the loop stable becomes a compromise with linearity improvement.

Integrated solutions have been in use for a number of years, but the requirements of low noise and high linearity offer a number of challenges to IC designers. Now, with modern IC processes, solutions offer performance and functionality that makes the adoption of the technique over more product areas increasingly attractive, opening the door for SDR transmitters.

The Cartesian Loop works to improve the linearity of a power amplifier device by the action of feedback. A block diagram of the scheme is shown in Figure 1. The input signal is required in in-phase and quadrature (I/Q) format. This is applied to a summing amplifier (usually know as the ‘error amplifier’) where it is compared to the feedback signal. The output of the ‘error amplifier’ is applied to an up-converter to generate an RF signal that is then amplifier by a power amplified. A sample output of the amplifier is taken, generally using a directional coupler; this is down-converted and applied to the error amplifier as described earlier. This forms the closed loop system, such that as



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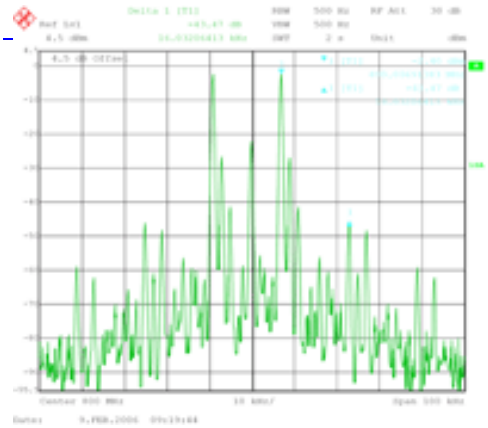
long as the feedback path does not introduce distortion, the system will attempt to correct the signal at the output to match the I/Q input signal applied to the error amplifier. The effectiveness of the solution is demonstrated in the results shown in Figure 2 where the upper trace is the PA operated without the feedback, and the lower trace is with feedback applied, in both cases the output power is approximately the same. It is obvious that the closed loop spectrum is a very substantial improvement on the non-corrected performance of the PA.

To achieve these results necessary to ensure the feedback phase is correct. This can be done by including a variable phase shifter in the LO path, typically to the down-converter, so that the relative phases of up and down conversion can be adjusted. This allows the desired feedback phase to be set. Also, it is necessary to include a means of constraining the loop bandwidth to ensure stability; hence a filter is included either around the ‘error-amplifier’ or immediately after it.

The Challenge

The need for the feed-back path to not introduce distortion places demanding requirements on the design in terms of linearity and noise. The need for low wide-band noise also makes the design of the up-converter challenging. Further, the

need for excellent isolation between up-converter and down-converter (as well as I and Q) makes the



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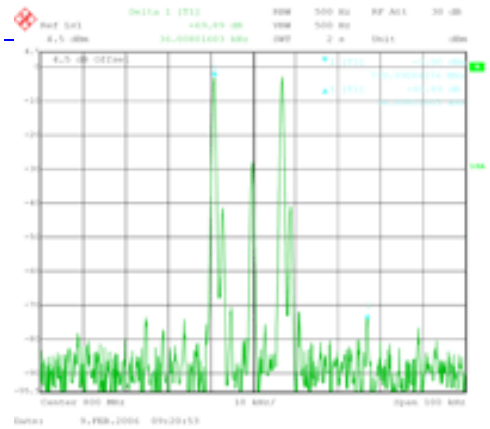
Cartesian loop a testing challenge for IC designers.

Traditional markets using CFBL solutions have been 25 kHz-channeled radios at 300 to 500 MHz. For some time manufactures have been demanding solutions operating up to 1 GHz while running from 3 V, taking less current than before and with no compromise on performance. One of the features of the specialized / professional radio markets is the diverse nature of the products and technologies employed, and while some manufactures are moving higher in frequency, many application are still operating at VHF leading to a demand for operation down to the 100 MHz.

To examine what can be achieved with a modern CFBL design we will use the CMX998 IC (ref [4]) as an example. The CMX998 represents a state-of-the-art solution for



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a flexible integrated CFBL design and is believed to be the first open-market IC solution to achieve all the objectives discussed above.

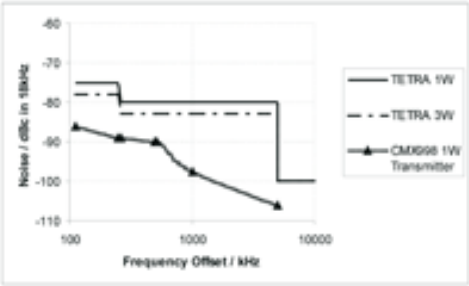
Typical Performance

The TETRA standard is a good benchmark for CFBL transmitters as it requires good linearity to achieve the required adjacent channel power levels of up to –60 dBc. Today the majority of TETRA terminals operate in the 300 to 500 MHz frequency range, but an increasing market is growing in frequencies around 800 to 900 MHz.

Although Cartesian loop technology has no problems operating at these frequencies, the availability of integrated solutions has been a major constraint on manufactures until now. One of the key advantages of the CMX998 is that it has taken the technology forward, so 900 MHz operation is now as easy as 400 MHz. This is demonstrated in Figure 3 and Figure 4. The plot in Figure 4 is a particularly impressive demonstration of the performance with adjacent channel powers of &#15063 dB / &#15064 dB representing a 28 dB improvement on the open-loop situation.

Wideband Noise

A key performance requirement for PMR standards such as TETRA is the wideband noise generated by the transmitter. This critically affects the ability of multiple terminals to operate in close proximity.



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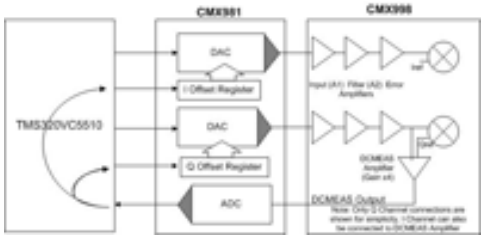
The TETRA standard states that transmitters must meet a noise mask that is evaluated using the TETRA channel bandwidth (equivalent to 18 kHz). The mask is more stringent for higher output powers to protect users on adjacent channels. The Cartesian loop is like any closed loop system in that noise inside the loop bandwidth behaves differently to noise outside the loop. Wideband noise, for example at a 5 MHz offset, is typically outside the loop bandwidth and is generally dominated by noise from the up-converter section. Closer to the carrier, e.g. at 100 kHz, noise is generated within the loop bandwidth, which is often dominated by the noise figure of the down-converter. The effect can be seen in Figure 5 where noise is relatively flat to about 500 kHz then rolls off quickly as the edge of the loop bandwidth is reached. By 5 MHz the noise is dominated by the broadband noise floor of the up-converter. Also shown on the graph are the TETRA 1 W and 3 W requirements, and it will be observed that the CMX998 based solution easily meets these requirements?

DC Calibration

The Cartesian loop is a DC coupled system, so any DC offset generated by the various amplifiers and mixers will have the effect of causing a DC error in the modulated baseband signal at the output of the error amplifiers. This, when applied to the up-conversion mixers, results in an increased carrier component in the RF signal (the so called



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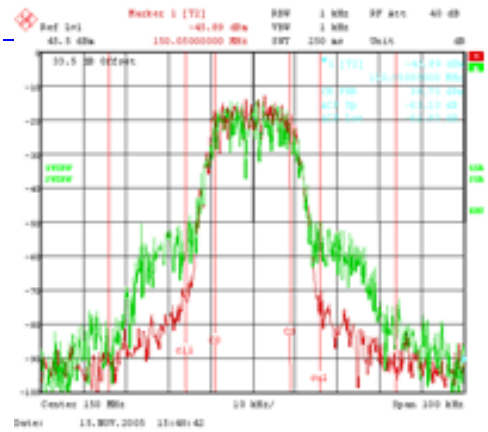
‘carrier leak’). If excessive, this will cause the intended modulation to be distorted so a method of removing the error is required.

Various solutions to the DC problem have been used over the years, but a simple and effective solution is a software controlled DC calibration loop. Figure 6 shows a test system used with the CMX998 which uses the DCMEAS output on the CMX998 to provide an error signal which is then sampled by the auxiliary ADC on the CMX981[5]. From the measured value a correction is computed, in the test system a Texas Instruments C55x DSP was used, and then the correction is loaded in the offset correction registers associated with the main Tx DACs in the CMX981. This results in a correction being applied to the I/Q inputs of the CMX998.

Adjusting the DC offset on the modulating IQ input signals can compensate for the cumulative error and thus the carrier can be nulled to better than &#15050 dBc if required. Calibration time depends on the accuracy of the required calibration, but typical numbers from the test system are around 300’s. Although a powerful DSP was used for convenience, the



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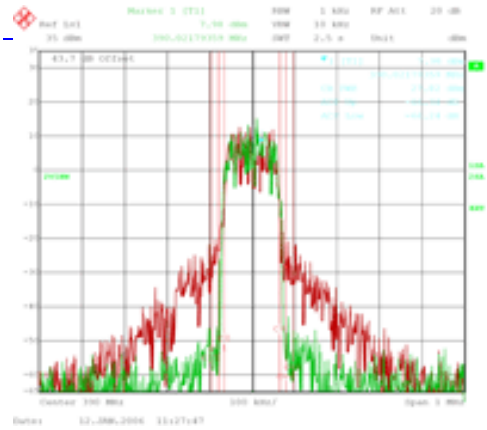
processing requirement of the correction algorithm is low, most of the time being spent managing communications to ADC and DACs.

Versatility

Today, manufactures are looking for versatile ICs with a common design that can be used in multiple products. An example of the versatility of the CMX998 CFBL solution is shown in Figure 7 where operation is at 150 MHz and the output power is 10 W mean, 30 W peak. The power amplifier used in these tests is a Toshiba PA module designed for FM operation (type: S-AV35,) but the CMX998 has no problem producing a clean transmit spectrum as can be seen in the lower trace on the plot.

It has already been stated that the Cartesian loop can support almost any modulation type. The loop is an analog system, it will reproduce whatever modulation is placed on the I/Q inputs, such as QPSK, GMSK, QAM, Analog FM, OFDM etc. One point worthy of note is that it is not easy to use the Cartesian Loop for peak limiting a signal. If Peak to Average Power Ratio (PAPR) reduction is required, this should be done prior to the CFBL. The reason is that the analog loop will try to reproduce the input precisely. This works well up until the maximum power the PA stage can deliver, at which point the CFBL will still try to increase the output power causing a limiting effect which leads to a broadening of the signal. As a result, limiting in the CFBL should be avoided.

A tough test of the flexibility of a linearization system is a two-tone test. Although the PAPR of a two-tone signal is only 3 dB, the fact the modulation has a zero (effectively goes through the origin in I/Q format) makes it a challenge for some linearization schemes, such as polar loop. As can be seen in Figure 4 the Cartesian loop deals with two-tone



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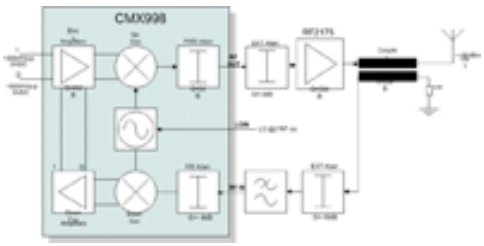
modulation very effectively.

Another aspect of the professional market is tough environmental requirements; to this end the CMX998 operates over a temperature range of &#15040&#176C to +85&#176C. The thermal environment for the CFBL IC can be severe, as it is often located close to the power amplifier that generates significant heat during transmission. With this in mind, the CMX998 uses a small QFN package, featuring excellent thermal properties due to the large ground pad specially added in the base. This helps keep the die temperature as low as possible benefiting performance. The QFN package also has the benefit of being physically small and has low-bond inductances, helping to enhance RF performance.

Future Technology – Broadband / Multicarrier / QAM

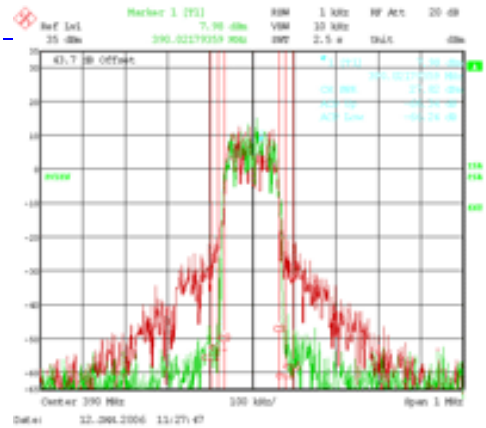
With the move to higher user data requirements, there is a general move to higher on-air bit rates. Often, this means broader bandwidth and higher-level modulations. The TETRA community is addressing this with the TETRA Release 2 which uses multi-carrier QAM modulation to achieve user bit rates of up to 500 kb/s. The TETRA 2 system can operate



[11]

on up to 150 kHz channels, but the transmitter must still meet the adjacent channel levels associated with a 25 kHz transmission. Wideband noise also must not be degraded.

To test performance for higher bit rate systems evaluation has been carried out using 16 QAM modulation, with a square root raised cosine filter, Bt = 0.2. For example, in a 50 kHz channel a QAM symbol rate of 38.4 kS/s can be used and in a 150 kHz channel a QAM symbol rate of 115.2 kS/s. These modulations are representative of broadband



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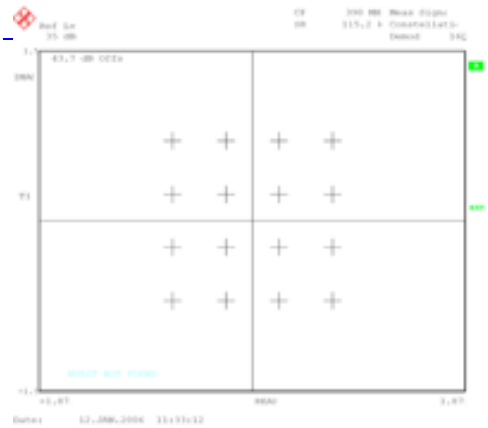
modulation, including a typically high peak-to-average power ratio of approximately 8 dB.

The results show the CMX998 can linearize systems with 150 kHz bandwidth signals very well, approximately 25 dB linearization can be observed in the plots. Results show that for both 50 kHz and 150 kHz QAM a 1st Adjacent Channel requirement of 55 dBc can easily be met.

To further demonstrate the flexibility of the scheme tests with GSM EDGE modulation, (8PSK) have shown excellent linearization. One of the main alternatives to the Cartesian scheme is ‘Polar Loop’, which has the advantage that low-noise phase modulators can be used, however the polar scheme is not as straightforward to implement as it first appears, and typical linearization gains are relativity small. For example, typical improvements in the adjacent spectrum may be only 6 dB to 10 dB. This compares with the 25 dB demonstrated in Figure 9 at 100 kHz offsets and beyond.

Cartesian loop can also be employed at higher frequencies by using up and down

mixing to a suitable IF. This scheme is a little cumbersome and does suffer from some



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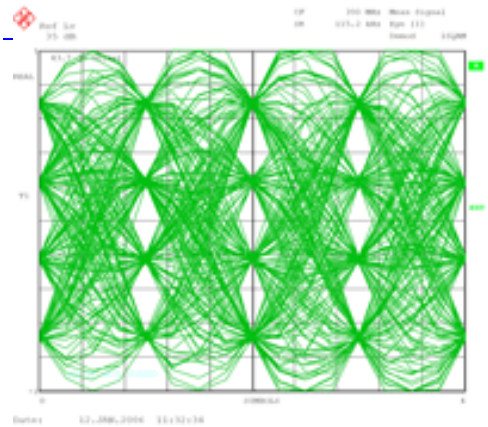
performance compromises; however, it is still an attractive option for some systems, such as portable satellite terminal transmitters that use QAM modulation. It has been found that mix-up / mix-down is often preferable to using discrete components to implement the loop directly at the operating frequency. This is because the CMX998 implements a whole range of functions: up-conversion, down-conversion, phase shifting, baseband amplification, gain control etc. A discrete solution may therefore require as many as six ICs to replicate the basic functions of the CMX998. This multiplicity of ICs often leads to layout and coupling problems to which the Cartesian Loop is quite susceptible; however, these can be largely avoided using an integrated solution. For example, the authors were involved in a discrete Cartesian loop design some years ago



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that took 3 engineers upwards of 6 months to design and optimize. The re-design of this circuit with an IC solution took one person two weeks.

Conclusion

We have seen that the CMX998 demonstrates a solution that fulfills all the key requirements of an SDR transmitter. The solution can be used over a wide-operating frequency range. Typically a product design is constrained by broadband local oscillator design and the availability of a suitable broadband power amplifier not the CFBL. Multiple modulation formats, excellent modulation accuracy and

flexible configuration are all achieved.

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