Reference Flow

Cadence Design Systems announces a 90 nm reference flow that addresses power-management and design-yield issues. The new flow is part of an ongoing collaboration with IBM and Chartered Semiconductor Manufacturing. The companies developed this design reference flow for the 90-nm low-power process technology on the IBM-Chartered Common Platform and to provide in solutions to accelerate time to market for system-on-chip (SoC) designs. The new RTL-to-GDSII reference flow is based on the Cadence&reg Encounter&reg digital IC design platform and enables high productivity and quality of silicon (QoS). The reference flow addresses low-power design challenges, from chip prototyping through power, timing and area optimization. The Cadence SoC Encounter GXL RTL-to-GDSII system enables timing-aware leakage power and dynamic power optimization, using power techniques such as multi-supply voltages, multiple-Vt optimization and clock gating. This optimization helps designers improve timing closure and reduce device area, while lowering power consumption. The flow addresses nanometer defect yield issues with yield analysis and optimization capabilities embedded in critical implementation stages such as physical synthesis and routing. For yield analysis, full-chip or block-level defect yield losses are assessed based on factors such as critical area and cell yields. A yield-prototyping capability enables designers to choose full-chip floor-planning strategies with visibility of yield considerations before committing to a physical architecture for the chip, allowing them informed design choices to speed yield ramp.

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