System-level and Transistor-level Simulation

Xpedion announces an interface to Simulink&reg from The MathWorks to couple system-level and transistor-level simulation for RF design. Designers will be able to use Simulink&reg in conjunction with Xpedion's GoldenGate RFIC Simulator to bridge the gap between system-level specifications and transistor-level performance. The current design methodology for advanced RFIC development starts with architectural tradeoffs made in Simulink. Once the specifications are developed, they are passed on to the RF designer, who is responsible to meet those specifications at the transistor level. Through the new design flow, designers can use the actual modulated signal, generated using Simulink, in GoldenGate, thus ensuring specifications are met.

Xpedion Design Systems

Source URL (retrieved on *02/01/2015 - 9:36pm*):
http://www.wirelessdesignmag.com/product-releases/2006/04/system-level-and-transistor-level-simulation