Digital RF and Handset Integration

Bill Krenik and Peter Rickert

As handset complexity continues to grow, the devices will be expected to incorporate an increasing number of mobile connectivity technologies, standards and applications without compromising performance. Increasing core component efficiency by using digital RF technology is an ideal solution.

Glossary of Acronyms

3D&#151 Three Dimensional

3G/4G&#151 Third/Fourth Generation

8- PSK&#151 8- Phase, Phase Shift Keying modulation

A/D&#151 Analog- to- Digital

A- GPS&#151 Assisted Global Positioning System

BiCMOS&#151 Bipolar Complementary Metal- oxide Semiconductor

CMOS&#151 Complementary Metal Oxide Semiconductor

DRP&#151 Digital RF Processing

DSP&#151 Digital Signal Processor

EDGE&#151 Enhanced Data GSM Environment

FIR&#151 Finite Impulse Response

GRPS&#151 General Radio Packet System

GSM&#151 Global System for Mobile Communications (formerly Groupe Speciale Mobile)

IC&#151 Integrated Circuit

IIR&#151 Infinite Impulse Response

IR&#151 Current Times Resistance, or Voltage

LAN&#151 Local Area Network

nm - Nanometer

OEM - Original Equipment Manufacturer

PA - Power Amplifier

PC - Personal Computers

Q- Quality Factor, referring to filters

SAW - Surface Acoustic Wave

SiGe - Silicon Germanium

SiP - System- In- Package

SoC - System- on- Chip

UMTS - Universal Mobile Telecommunications Service

Concerns about board space, power consumption and cost in relation to mobile device design have grown in importance as consumers increasingly view their mobile phones as portable home entertainment centers. Although today's phones are expected to process far more than the simple voice phones of yesterday, users demand ever— increasing battery life and smaller form factors. As 3G, 4G and

beyond expand the data highway, this trend will only accelerate.

It's about Integration

Perhaps the best opportunities for handset designers to add the functionality consumers want without increasing board space requirements, power consumption or cost, lie in the RF components built into every handset. As analog devices, these components occupy comparatively large amounts of space, sometimes as much as half the board, and consume significant power. The board space they need may be so great that adding radios becomes almost impossible without increasing the overall form factor when Bluetooth, broadcast TV reception, A— GPS, wireless LAN and other functions are built into the handset. Power consumption and cost also increase with the addition of each set of RF components. Until recently, makers of advanced handsets have been forced to reckon with unpalatable trade— offs in size and cost as they added greater and greater functionality to mobile devices. (See Figure 1.)

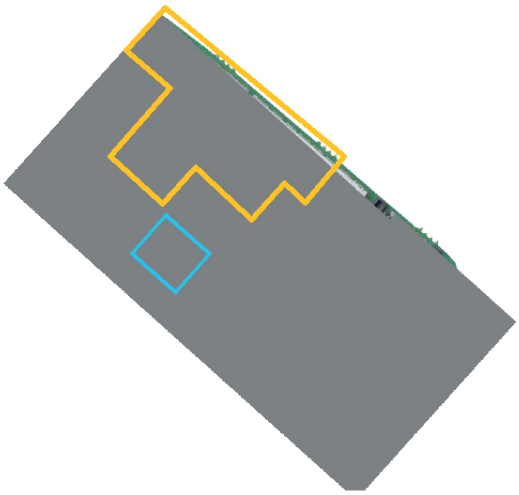
It is critical to address this dilemma with technology that helps designers increase functionality without adding components to the handset. The focus is to put core components to work more efficiently, allowing the handset to perform more radio— based operations with only marginal increases in board space requirements, power consumption and cost.

Texas Instruments' DRP technology&#153 moves in this direction with board space, power and cost economies that have sweeping implications for wireless handset designers. The intent of DRP is to move the A/D and D/A conversions as close to the antenna as possible and to perform all processing except initial filtering in the digital domain. This approach allows increased performance while cutting board space requirements, silicon area and power consumption roughly in half. (See Figure 2.)

SoC and SIP Mainstays

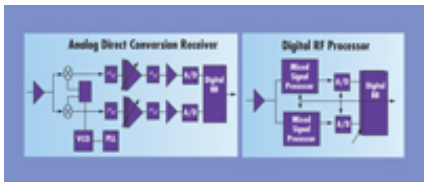
In wireless handsets, many designers use both SoC and SIP technologies. Because it allows stacking of semiconductor devices to conserve board space, SIP often proves the best approach to the RF front end. PAs, SAW filters, RF switches and their associated passive elements are best implemented as SIP modules. On the other hand, considerable benefits are gained from SoC integration of the RF transceiver function with the system baseband processing function in deep sub— micron CMOS.

RF SoC integration can reduce power, cost, board area and test cost while improving performance, measurement, phone manufacturing and yield.



[1]

[2]



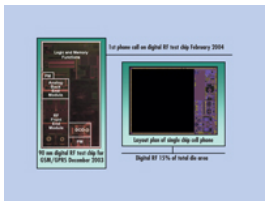
[3]

Given the tremendous logic density and high clock speeds offered by deep submicron logic processes, it seems natural to look for ways to exploit this process technology through SoC. Doing so may require developing new radio architectures for implementation in deep submicron CMOS, but it can provide significant advantages to the designer. Foremost among them is the fact that, as advances in CMOS wafer processing produce faster switching speeds, it becomes possible to sample at higher rates.

Oversampling of the input signal reduces noise aliasing problems and relaxes the design of the input networks. More complex filtering can be added and A/D conversion can take place closer to the antenna. In addition, SoC integration improves system yield because more of the system function is implemented as logic (vs. analog RF which suffers parametric yield loss). Moving the radio function to an aggressively scaled technology also reduces board area and total IC silicon area.

Because digital radio requires few passive elements, board real estate requirements may be reduced dramatically by integrating the transceiver and digital baseband processing functions. And although highly integrated SoC devices sometimes cost a little more than less sophisticated alternatives, fewer devices generally are needed and, as a result, design, test and debug costs may drop significantly. An important side benefit is that lower design complexity often results in faster time to market.

Power requirements shrink, to a certain extent, when the number of devices in the system is reduced. However, greater power benefits derive from the fact that digital logic is quite low power and that the CMOS process is inherently less power—hungry than other processes, such as SiGe BiCMOS, customarily deployed for analog devices. It's worth noting, too, that 90 nm CMOS technology is available today, 65 nm is sampling now and 45 nm is down the road a ways. Such small geometries are not available in SiGe BiCMOS. In fact, most SiGe radios today are still 180 nm. (See Figure 3.)



[4]

[5]

Development of Digital RF

Only within the past few years has digital CMOS been able to clock fast enough and at a power low enough to permit digital processing in the RF domain. For digital RF, clock speed must equal the radio frequency, which, in Bluetooth for example, can be as high as 2.4 GHz. Today, PCs and DSPs clock at that rate, or even faster. As a result, it now is possible to gain the advantages of digital processing in wireless RF components.

Digital processing, of course, may be scaled readily as process technologies grow more refined. But the radio still has some analog circuitry, and removing that will require new radio architectures and moderate redesign. In general, though, the radio will move readily from one process node to the next because it is largely digital.

DRP Advantages

DRP designs move some of the functions from the analog domain to the digital domain to overcome some of the stringent requirements for the analog and RF blocks, which make SoC feasible with 90 nm or 65 nm CMOS. Most components needed for analog and RF integration, such as resistors and capacitors, can be leveraged with the standard CMOS flow for low cost and high function integration. (See Figure 4.)

One advanced method uses copper for interconnect. Its high conductivity offers opportunities to integrate passive components such as inductors and capacitors. Innovative 3D capacitor design, using multi— level interconnect, offers high capacitance density for area reduction. Thick top metal, needed for the digital power bus to minimize IR drop, also enhances the Q of the integrated inductor.

Very fast RF CMOS components enable circuit designers to eliminate certain tight analog filters entirely. Most filter functions can be done digitally, a shift that reduces power consumption and area. RF CMOS components require only small amounts of energy to turn on/off a fixed ohm linear switch, which is a great enabler for switched capacitor circuits, mixers, switching mode supplies, pass devices of regulators and class D amplifiers as well.

One methodology that helps eliminate the need for high performance passive elements involves sampled data techniques. The sampling operation naturally gives rise to frequency translation. Consequently, signal down— conversion is easily achieved. Once the input waveform has been captured on sampling capacitors, it is

easy to combine charge samples.

Multiple samples of a waveform taken on the same capacitor allow implementation of a simple moving average filter. More complex FIR and IIR filters also can be realized easily. A/D conversion can be achieved through a variety of techniques, and digital signal processing can be used to further process the signal.

As CMOS process switching speed increases, it becomes possible to sample at higher rates. Oversampling of the input signal reduces noise aliasing problems and relaxes the design of the input networks. More complex filtering can be added and A/D conversion can take place closer to the antenna, moving more of the signal processing burden to the digital domain, where the full benefit of logic scaling is realized.

When the design rules become tighter at the 65 nm node, the technology faces several challenges. The increase in parasitic resistance because of narrower source/drain regions, smaller gate lengths, smaller contacts and higher aspect ratio of vias all contribute to potential degradation of the devices. However, new silicided materials are used to obtain lower contact resistance and reduce parasitic source/drain resistance, the contact resistance and gate resistance. This virtually eliminates performance degradation.

The Future of DRP

Developing digital RF solutions for A— GPS, digital TV, Bluetooth wireless LAN, UMTS and other air interfaces is not without challenges. Wireless LAN requires wider bandwidth. EDGE involves 8— PSK modulation. Wideband CDMA imposes various requirements for linearity over a 5 MHz band. However, advanced DRP technology provides a means to meet these challenges as the wireless industry's needs require. (See Figure 5.)

Smaller process geometries will facilitate development of digital RF solutions and of single— chip solutions for these and other systems and standards. There are already plans to migrate DRP to the 65 nm process node. Moving to the next smaller process node also presents unique challenges. Closely linking process technology development and chip design methodology early in the development cycle is critical.

Before long, analog RF will virtually disappear from the wireless landscape as OEMs move to increasingly sophisticated handsets incorporating multiple radios to deliver widely varied applications. CMOS technology will dominate the RF domain as semiconductor makers move to smaller process nodes. SiGe BiCMOS will continue to be found in high performance equipment such as radar and some microwave systems. This process may also continue as useful technology for cellular basestations. (See Figure 6.)

RF circuitry will become a key driver for CMOS process technology. Dealing with noise, isolation and passive element performance in the RF becomes more important as smaller process nodes become more common. Process logic density and logic speed also are important drivers of CMOS development.

For wireless handsets with the multiple radios needed to deliver the functionality that consumers expect, DRP clearly is the path to the future. Software— defined radio will be important in using radio components efficiently and in reducing the total number of radios needed. But there can be no question that board space considerations, if nothing else, will mandate the move to more compact RF. Power concerns and cost will add impetus to this shift away from analog RF processing.

Though different designers may choose different integration schemes &#151 integration of the transceiver with analog or with digital components, for example &#151 in the near term, the long range view suggests that wireless signals will be processed almost entirely in the digital domain. An incoming signal will pass through the antenna, a switch and a filter. Digital sampling will occur as the signal comes out of the low noise amplifier. Some mixed signal processing may be required at that point. From then on, though, everything is digital. That's the future.

About the Authors

Bill Krenik is Wireless Advanced Architectures Manager for the Wireless Terminals Business Unit, Semiconductor Group for Texas Instruments. Dr. Krenik has been employed by TI since 1985. Dr. Krenik received a PhD in electrical engineering at the University of Texas. He also received an MSEE at Southern Methodist University and a BSEE from the University of Minnesota. Dr. Krenik is a senior member of the IEEE and he is a registered professor of engineering in Texas. He holds 29 U.S. patents.
Peter Rickert, P.E., is a TI Fellow and currently responsible for the Platform Technology Development for the ASP and WTBU organizations at TI. He has held multiple engineering and management roles across TI during his 25— year career.

Rickert received his BSEE at Clarkson University in 1980. He became a Registered Professional Engineer in Texas in 1992 and is a senior member of the IEEE.
oeb e aecg f

Source URL (retrieved on *03/14/2014 - 8:11am*):
http://www.wirelessdesignmag.com/product-releases/2005/11/digital-rf-and-handset-integration

Links:
[1] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0511/wd511_f1_1.jpg
[2] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0511/wd511_f1_3.jpg
[3] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0511/wd511_f1_4.jpg
[4] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0511/wd511_f1_5.jpg
[5] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0511/wd511_f1_6.jpg