Designing a Dual-band LNA for Wireless LAN Applications

As receiver technology drives to become more integrated and receivers become more sensitive, LNA designs feel the pressure to meet tough new specifications.

By Zulfa Hasan-Abrar and Yut H. Chow

Highly integrated, cost-effective RF circuitry is becoming an essential element for the ubiquitous operation of portable wireless equipment. The receive circuitry sensitivity is critical to the range over which the wireless network can operate. In particular, the LNA plays an important role to ensure stable reception of signals.

This article will discuss the design and implementation of the MMIC and module level circuitry of a dual-band LNA that operates in the IEEE 802.11g/a bands. The complete LNA is housed in a 3 &#215 3 mm molded chip-on-board package and requires only two external bypass capacitors for operation.

The dual-band WLAN LNA operates at 2.4 GHz (802.11b/g standard) and 4.9 to 5.95 GHz (802.11a standard) bands. The LNA is designed using ADS EDA software and is fabricated using an enhancement-mode pHEMT GaAs process in a 3 &#215 3 mm plastic package.

The Dual-band LNA

A typical dual-band LNA, designed for the IEEE 802.11g/a bands, is required to operate with low current and high gain. Further, it must exhibit a low NF over both the 2.4 GHz and 5 GHz bands.

In addition, the 5 GHz amplifier must cover a 4.9 to

5.9 GHz since different countries operate the 5 GHz band at slightly different frequencies. This implies the LNA must maintain a constant operating performance across a 20% bandwidth. Table 1 summarizes the key specifications for the LNA in both bands.

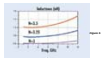
It is obvious that the specifications are extremely challenging technically. In addition, the specifications must meet high-yield and high-volume manufacturing.

Figure 1 shows a typical on-wafer plot of an 800&#181m FET NF_{min} in an enhancement-mode pHEMT GaAs process across different bias conditions. Measurement uncertainty is about 0.05 dB. The noise performance is outstanding.

Simulation models were extracted for different device sizes that incorporate noise, small-signal, and large-signal characteristics. Accurate results were obtained using the Root model in the ADS design suite. The model is scalable in size and usable over wide bias ranges. This is important, as the designer will need to sweep size and bias to find the optimal design solution.

2.4 GHz LNA Design

A cascode topology is used in the 2.4 GHz LNA because it gives higher gain due of the absence of Miller capacitance, and it permits current reuse in what is effectively a two-stage design. In addition, the cascode configuration enables higher linearity to be obtained for the same current draw (see Figure 2).



Q1 and Q2 form the gain and cascode FET pair. Inductor L2 and capacitor C2 form a L-C resonator load used to resonate the cascode transistor output at 2.4 GHz. Source inductance to ground at Q1 acts as a series feedback to simultaneously improve input match and NF. The input impedance at Q1 gate can be approximated by Equation 1.

In the equation, g_m is the transconductance of Q1, and L_s is the total source inductance at the source of Q1. In practice, this is the sum of bond wires connected to the die and via hole inductances in the PCB. L3 is an additional off-chip SMT component, to match the input of the LNA as close as possible to the minimum noise figure impedance Γ_{opt}. Capacitor C3 acts as an RF bypass for Q2. Capacitors C1 and C8 are DC blocking capacitors. FET Q4 is a current mirror for biasing, resistive voltage dividers R1 and R2 set the gate voltage for Q2 and FET Q3 acts as a shutdown switch. To model the non-idealities of a surface mount component, S-parameter data from the manufacturer were used.

At 2.4 GHz, the effects of parasitics, such as spiral inductor losses and the mutual coupling of bond wire inductances, can affect performance significantly. For example, the L-C resonant tank at the Q2 drain is implemented on-chip and therefore needs to be modeled rigorously. 2.5D E-M simulations were performed on Momentum over as large of a circuit coverage as possible. The results of the spiral inductor simulations are shown in Figures 3 and 4.

Figures 3 and 4 show the plot of inductance and Q factor vs. the frequency and number of turns. These simulation results were used with the circuit level components to simulate the complete LNA. Without optimizing the circuit, the result already shows that gain peaks correctly at the center frequency of 2.4 GHz. Series resistance along the inductor is the manifestation of the skin effect that occurs on the inductor metallization at high frequency. Gain, noise figure and return loss all still meet the specifications. Further optimization on ADS shows performance can still be improved. Figure 5 shows the performance of the LNA after the components value has been optimized.

5 GHz LNA Design

Unlike the 2.4 GHz LNA, the 5 GHz LNA requires higher gain that must be flat for more than 20% of the bandwidth at the 5 GHz band, and a noise figure that is tightly controlled in-band. A two-stage amplifier is required to meet these specifications (see figure 6).

This amplifier again employs inductive loading (L2 and L4) at each of the stages, both of which are integrated on-chip. Input impedance and noise matching is again achieved in a similar manner as with the 2.4 GHz version, with a source inductor and shunt input inductor at the gate. A shunt R-C feedback (R10 and C3) is used in the second stage to improve the output match. Components L3 and C2 form a highpass interstage match. This match compensates for the negative gain roll-off from the first stage so that the overall gain forms a bandpass response centered at 5.5 GHz. Capacitor C3 acts as an RF ground for the matching network. The R-C network across C3 (R4 and C4) improves the stability of the amplifier. The Q2 source is grounded through a backside via.

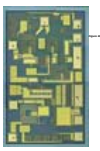
ADS enables different models to be used to model non-ideal characteristics of the passive components. Bond wire coupling is significant in the 5 GHz design, and the various models enable coupling to be modeled with sufficient accuracy to mimic actual performance.[1] Figure 7 shows the simulation result of the complete 5 GHz band LNA with (a) ideal components and (b) optimized non-ideal components value.

Note the significant effects on S_{22} and the shift in gain peaking with non-ideal models simulated in Momentum. A more complete Momentum simulation would be to simulate the complete layout in Momentum and add active devices later to the multiport s-parameter file generated by Momentum. This is shown in Figure 8.

Simulation results reveal that inductive coupling significantly affects frequency response. It also highlights regions of high current densities that can affect P1dB performance. The complete simulated results are shown in Figure 9. Figure 10 shows the die picture of the complete dual LNA.

The measured vs. simulated results for both of the dual-band LNAs is shown in Figures 11 and 12. The discrepancies are a result of die-level and PCB ground interaction and the effects of plastic molding compound over the chip. These serve to shift the frequency response curves and de-Q the circuit components, the effects of which are most pronounced in the S_{22} response and the high frequency gain curves. Despite these, the responses peak at the values that correspond to the WLAN frequency bands with outstanding noise and gain performance.

Conclusion

As with all designs, a dual-band WLAN LNA requires trade-offs. EM simulations together with circuit level simulation tools are indispensable for compact designs. In the 2.45 GHz band, gain is 17 dB at 14 mA current with 0.9 dB NF. In the 5 GHz band, gain is 22 to 24 dB at 22 mA and 1.5 dB average NF. 

Input P1dB is &#150 5.5 dBm for the 2.4 GHz LNA and typically &#150 14 dBm for the 5 GHz LNA. IIP3 is +5.5 dBm for the 2.4 GHz LNA and typically &#150 2 dBm for the 5 GHz band. The complete design uses only one RF input matching component external to the MMIC inside the module. The complete LNA is housed in a 3 &#215 3 mm molded chip-on-board package and requires only two external bypass capacitors in actual operation.

Endnote

1. A.O. Harm, K. Mouthaan, E. Aziz, and M. Versleijen, &quotModeling and Simulation of Hybrid RF Circuits Using a Versatile Compact Bondwire Model,&quot *Proceedings of the European Microwave Conference*, pp. 529-534, Oct. 1998, Amsterdam.

About the Authors

Zulfa Hasan-Abrar and Yut H. Chow are employed at Agilent Technologies (Malaysia) in Penang where they are engaged in the R&D of GaAs MMIC ICs. They can be reached at Agilent Technologies (M) Sdn Bhd, WSD R&D, Phase III, Bayan Lepas FIZ, Penang 11900, Malaysia.

Source URL (retrieved on *07/24/2014 - 6:59am*):
http://www.wirelessdesignmag.com/product-releases/2005/10/designing-dual-band-lna-wireless-lan-applications?qt-digital_editions=0

Links:

[1] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_1_lrg.jpg
[2] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_table_lrg.jpg
[3] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_2_lrg.jpg
[4] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_3_lrg.jpg
[5] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_4_lrg.jpg
[6] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_5_lrg.jpg
[7] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_6_lrg.jpg
[8] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_7_lrg.jpg
[9] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_8_lrg.jpg
[10] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_9_lrg.jpg
[11] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_10_lrg.jpg
[12] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_11_lrg.jpg
[13] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/0510/wd510f1_12_lrg.jpg