An Innovative Approach to Faster RFIC Transmitter Design

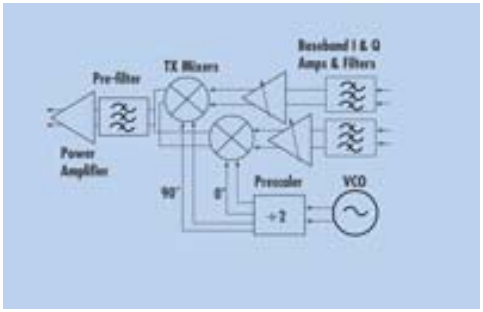
Transmitter designs continue to evolve at a blazing pace, in both complexity and integration. In today's competitive wireless environment, accurate and efficient transmitter design isn't an option — it's a must.
By Andy Howard

RFIC transceiver design requires many simulation technologies and capabilities. This article presents a number of simulation techniques, including frequency-domain (harmonic balance); mixed frequency- and time-domain (circuit envelope); electromagnetic; and mixed numeric-, frequency-, and time-domain (wireless test benches), applied to the transmit portion of an integrated RFIC transceiver for WLANs and IEEE 802.11b. These simulation techniques usually are fast and efficient, and should be of interest to RFIC designers still using traditional time-domain simulators.

Background

The direct-conversion transmitter consists of a VCO with prescaler to generate differential-mode quadrature LO signals to drive the I and Q mixers. Analog, tunable baseband filters and amplifiers are included on-chip, as well as the relatively low-power amplifier. A block diagram of the transmitter is shown in Figure 1.

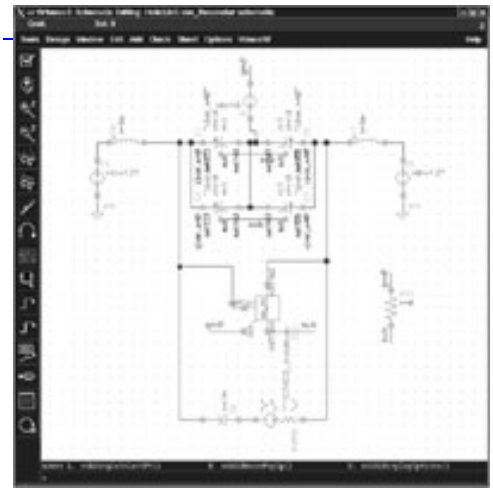
For this design process, assume a system designer has done a top-level design using behavioral models and has handed down rough specifications for each block to the RFIC designer. The RFIC designer may have an existing design for a different frequency range, power output, operating efficiency, and manufacturing process. So it is assumed the designer will start by converting each block in the design to the target manufacturing process. It will be necessary to adjust the design (primarily bias voltages, currents, and device sizes) of each block to achieve basic functionality. Then, further investigation and design may be necessary to ensure that they meet the required level of performance, and also to "explore the design space" to see if better performance at a lower cost (power consumption and area) can be achieved.



[1]

There are a number of questions the designer will have to address during the design process: Will the VCO oscillate, and over what frequency range? What is its tuning characteristic? What about phase noise? How do the VCO's characteristics vary with temperature? Is the prescaler output signal sufficient to drive the mixer? Will the VCO continue to oscillate when connected to the prescaler? How does the conversion gain of the mixer depend on the LO signal amplitude? How do you improve the mixer's third-order intercept point? How does it vary with bias current? Can it be optimized? How does the mixer distort signals with WLAN modulation? Similar questions concerning the baseband chain and power amplifier also must be addressed.

For efficiency, it is important that EDA tools used during the preliminary design process enable designers to easily sweep, tune, or optimize parameters that directly affect the important responses of their circuits. Also, it is important that the tools enable designers to view the simulation results clearly and with flexibility, to enable them to gain insight and clearly document results.

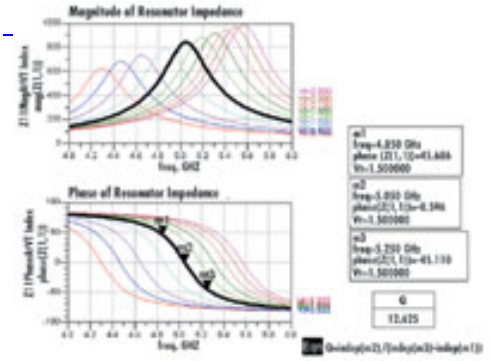


[2]

The majority of the responses of interest for the circuit blocks in the transmitter may be computed directly from the frequency domain spectrum while the block is driven by a small number of sinusoidal tones. So it makes sense to use frequency-domain simulation tools, provided they can handle the complexity of the circuits. Frequency-domain tools are able to solve more complex circuits than one might

think. Frequency-domain simulators have the added advantage that they can handle frequency-domain models and measured data directly, without requiring that some lumped equivalent circuit be generated.

Simulating complex, modulated signals, such as WLAN and WCDMA, in modern communication systems requires more than frequency-domain simulation. This is because frequency-domain simulation is only for steady-state responses, whereas complex, modulated signals vary randomly with time. There are several ways of simulating such modulated signals that will be shown later.



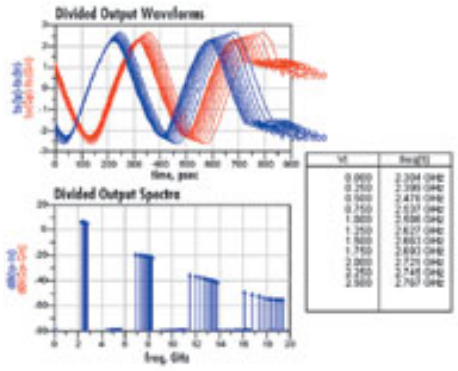
[3]

Applying Frequency Domain Simulation in the VCO Design

Two initial important characteristics of VCO design are determining the range of resonant frequencies of the tunable resonator, and whether the circuit will oscillate or not.

One method starts with a resonant circuit, including the varactor diodes and an ideal inductor replacing the spiral. Running a frequency-domain S-parameter simulation with the tuning voltage swept as a parameter gives the resonator tuning range. Adjusting the inductance value and/or the size of the varactor diodes allows the tuning range of the resonator to be set.

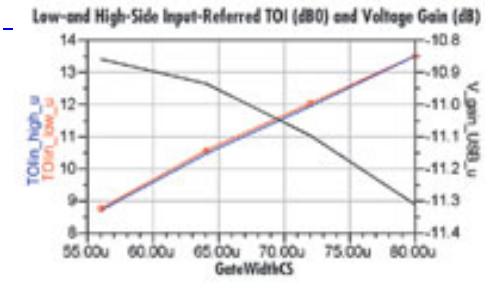
Once the resonator operates in the desired tuning range, replace the ideal inductor with a planar spiral with the same nominal inductance. A planar electromagnetic solver tool may be used to simulate the spiral inductor and generate an accurate frequency-domain model that can be used in all subsequent simulations of the VCO. Figure 2 shows a simulation setup for testing the tuning range of the resonator. Figure 3 shows the resonator frequency response and tuning range, with tuning voltage swept as a parameter.



[4]

What if the VCO doesn't oscillate? How can simulation tools be applied to determine why, and to resolve the problem? Half of the VCO design concerns the resonator, and the other half concerns the active circuit that generates a negative resistance over some frequency range that is large enough to overcome the losses in the resonator. If the simulator indicates the VCO will not oscillate, the process to analyze it involves removing the resonator, replacing it with a test signal, sweeping it versus frequency and/or amplitude, and using it to determine the impedance presented to the resonator. If the real part of this impedance is not negative, or its magnitude is too small, experimentation by adjusting bias currents and device sizes until the conditions for oscillation are satisfied is the required process.

Once the VCO is operating, verify its continued oscillating state when connected to the prescaler and over the desired frequency range. Figure 4 shows the output of the prescaler, when driven by the VCO, as a function of the tuning voltage.



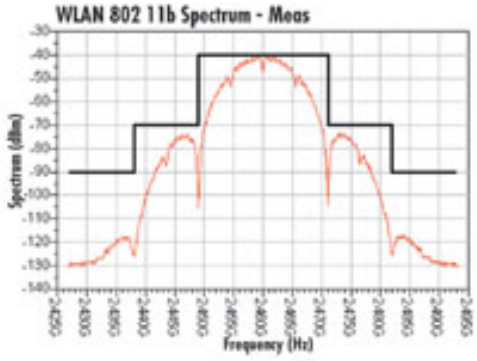
[5]

Also, verification that the VCO/prescaler combination operates over temperature and manufacturing process variations is required. These simulations can be realized by selecting a tool that easily solves VCOs and prescalers versus swept parameters. Frequency-domain simulators (given a transient-generated initial guess when solving prescalers) are particularly well-suited to this type of swept simulation, when assessing the steady-state response of a circuit versus a parameter. This is because when running parameter sweeps, the frequency-domain simulator uses the solution of the circuit for swept parameter value the n^{th} — 1 value of the swept parameter as an initial guess to solve the circuit with the nth value of the swept parameter. Solutions are found quickly and easily, provided the circuit's response

does not vary too rapidly relative to the variation in the swept parameter.

Applying Frequency-domain Simulation to the Mixer Design

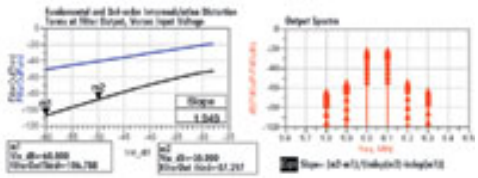
In direct-conversion systems, mixers are usually used to convert signals from RF to baseband (in the receiver) or from baseband to RF (in the transmitter). Mixer specifications such as conversion gain and IP3 may be computed directly from the steady-state frequency-domain spectra of the input and output signals. The larger the ratio of the output to the input frequency (and this ratio can be particularly large for direct-conversion systems because the baseband is near DC), the longer the simulation time required, if a purely time-domain simulator such as SPICE is used. This is because with a time-domain simulator, a time step small enough to sample the RF and its harmonics and a stop time long enough to capture a full period of the lowest frequency signal must be used. Frequency-domain simulators do not have this frequency-ratio problem, as the simulation time required is not dependent upon the frequencies of the signals.



[6]

When characterizing mixers (as well as other blocks in the design) and optimizing their performance, it is useful to be able to sweep and optimize parameters. With frequency-domain simulation, the performance characteristics targeted for improvement may be plotted versus an arbitrary swept parameter, or may be optimized directly. It will be easy to see, for example, voltage conversion gain vs. LO drive amplitude and determine how large the output of the prescaler needs to be. It will also be easy to see conversion gain vs. input signal amplitude, which will indicate how large the baseband signal may be before compression becomes unacceptable. Figure 5 shows the trade-off between voltage conversion gain and third-order intercept point, as the gate width of one of the devices (which sets the bias current) is swept.

With these parameter sweeps, designers should have a rough idea which parameters will most strongly affect the voltage gain and the third-order intercept. But if these parameter sweeps may be carried out quickly (in this case, sweeping a FET width to four different values and calculating conversion gain and IP3 required only 75 seconds), then it is easy to determine which parameters matter and which do not.

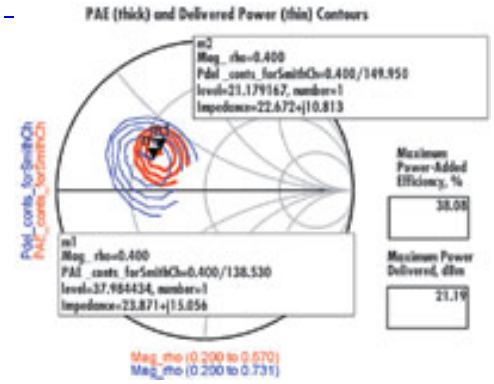


[7]

An optimization allows the designer to vary multiple parameters simultaneously while attempting to improve different performance characteristics. In this case, different device FET widths were varied to maximize conversion gain and IP3 simultaneously. To test the robustness of the optimizer, the initial parameter values were intentionally set to give poor performance. In less than 25 minutes, the optimizer improved the IP3 point by about 14 dB and the voltage conversion gain by more than 3 dB.

How Blocks Distort WLAN Signals

Mixers and other blocks are traditionally characterized and specified using sinewaves. But the sinusoidal specifications (typically gain compression and IP3) may not predict adequately the performance degradation that each block will introduce when it handles complex, modulated signals. To carry out such simulations requires:
• Numeric processing capability to generate the signals.
• The ability to convert them into time-varying signals that a transistor-level simulator will be able to handle.
• A mixed frequency- and time-domain simulator to efficiently handle both high frequency RF signals and relatively slowly varying modulation signals.
• The ability to quickly characterize circuit behavior and create models that may be simulated much more efficiently than transistor-level circuits.
• Prepared templates to display the results such as EVM, spectrum, peak and average power, and constellation diagrams.



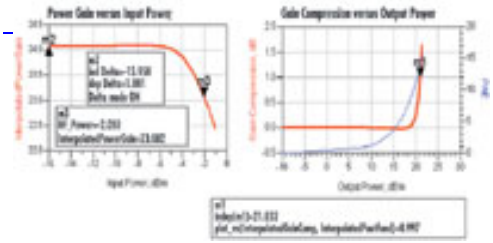
[8]

The tools used for simulating WLAN signals are based on the Ptolemy simulator from UC Berkeley: numeric processing, co-simulation (which carries out simultaneous numeric processing and transistor- or behavioral-level simulation), circuit envelope (for mixed frequency- and time-domain simulation), automatic

verification modeling (for fast model generation from an automatic swept power frequency-domain simulation), and data display. These have been combined together into a "Wireless Test Bench," so it isn't necessary to be a wizard in all the underlying tools and techniques to get useful results. Figure 6 shows the mixer's output spectrum and that the WLAN spectral mask requirement is satisfied.

Applying Frequency-domain and WTB Simulation to the Baseband Chain

Baseband analog circuits have traditionally been simulated with time-domain simulators such as SPICE. But there is no reason that frequency-domain simulation cannot be applied to them as well. The same type of gain and IP3 simulations may also be run in the frequency-domain on the baseband circuits, except without frequency conversion.



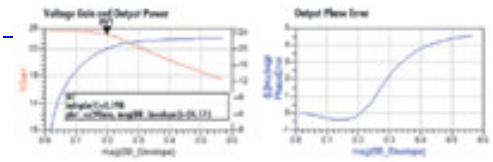
[9]

An attempt was made to characterize the non-linearity (IP3 point) of the baseband chain (Gm-C filter[1] and variable gain amplifier). However, because of the filter structure, it does not have traditional third-order nonlinearity. This may be seen from a two-tone, swept amplitude simulation, and a plot of the resulting fundamental and third-order intermodulation distortion tones vs. input signal amplitude, as shown in Figure 7.

The intermodulation distortion tones do not rise at a 3-to-1 slope, indicating that no IP3 point may be calculated. In this case it is better to use the Wireless Test Bench simulation to see to what extent the baseband chain distorts signals. Using this approach shows that the EVM introduced by the baseband chain is strongly dependent upon the bandwidth of the filter, and that if it is even just several MHz too narrow, the EVM rapidly degrades to an unacceptable level (from 15% to 25%).

Simulating the PA

More could be said about simulating the PA, but the following information highlights a few aspects. In this design, the PA is integrated with the rest of the transceiver and is used for a relatively low output power WLAN (802.11b) application.

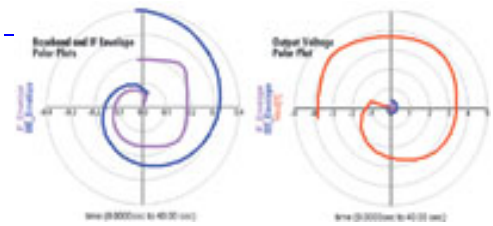


[10]

Parameter sweeps and rapid frequency-domain simulation enable efficient load- and source-pull simulation of the active device(s), which should indicate optimal load and source impedances (and harmonic impedances, if desired) for maximizing power delivered and/or power-added efficiency. Figure 8 shows load pull simulation results for one of the FETs used in the output stage of the PA.

Once the optimal impedances are determined, spiral inductors are likely to be required to achieve them. As described earlier, electromagnetic simulation of the planar spiral structures will produce highly accurate models that may be simulated very efficiently in the frequency domain. A one-tone swept power simulation beyond the 3 dB gain compression point requires only about five seconds. A two-tone swept power simulation of the IP3 point requires only about 30 seconds.

The next step is to create an extracted view of the amplifier, which has more than 250,000 parasitic elements (including 754 nonlinear — in this case, using the Cadence AssuraRF tool). Using the same harmonic balance frequency-domain simulator as above, a one-tone power sweep simulation of this extracted view to beyond the 1.5 dB gain compression point requires about two hours and 38 minutes, indicating that harmonic balance is able to handle extremely large circuits. Figure 9 shows the extracted view simulation results.



[11]

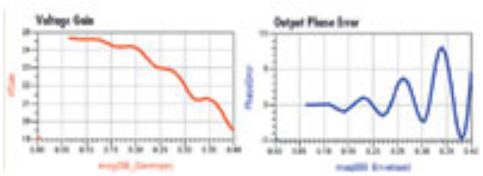
A Wireless Test Bench simulation (requiring about 40 seconds) was run on the amplifier (but not the extracted view), to determine the maximum input power that could be supplied while still satisfying the output spectral mask requirement.

Simulating the Overall Transmitter

A final test verifies the performance of the overall transmitter design. The tests are described with all blocks modeled at the transistor level.

The first simulation is a slow sweep of the baseband I and Q signal amplitudes at the inputs to the I and Q baseband chains. Ideally, the amplitude of the signal at the output of the PA should linearly track the magnitude of the vector created by the combination of the I and Q inputs. Any deviation from linear in the amplitude and any change in the phase of the output signal is distortion.

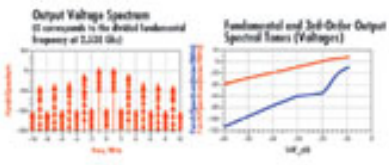
The designer should evaluate voltage gain as well as phase variation at different locations in the transmitter to determine where the distortion is being introduced. Alternatively, the designer could ensure that the baseband signal amplitudes are below the levels at which output phase and magnitude distortion become unacceptably large.



[12]

Even though this simulation is large, with a schematic view having nearly 3,500 devices, of which more than 1,500 are nonlinear, it requires only eight minutes and 20 seconds, after a one-time simulation of six minutes and eight seconds, to establish an initial guess. Figure 10 shows the simulation results, and indicates that provided the magnitude of the vector made from the baseband I and Q signals is less than about 0.25, the gain compression and phase error are quite small.

It is also possible to sweep both the magnitudes and phases of the I and Q baseband signals such that the resulting magnitude and phase of the amplifier output signal sweeps out a spiral. Figure 11 shows the baseband input spiral, and the spiral at the output of the baseband chains (labeled "IF," even though there is no frequency translation) on the left, and the spiral at the output of the PA, on the right. Notice that the spiral already shows compression before any RF processing. This enables a fast way to test how well many baseband I and Q combinations map to the RF output signal. The required simulation time varies with the resolution of the spiral that is created, but the coarse spiral shown in Figure 11 only required about ten minutes.

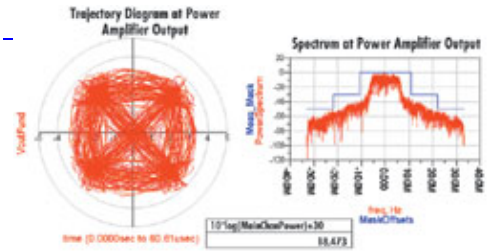


[13]

A double-sideband modulation test is carried out with both I and Q input signals being in-phase sinusoids at 1 MHz. The VCO is set near 5 GHz, giving an LO near 2.5 GHz. The output of the PA has a double-sideband spectrum centered at the LO frequency. The amplitudes of the baseband sinusoids can be swept showing a corresponding increase in intermodulation distortion. This simulation requires one hour and 19 minutes, somewhat longer than the simpler modulation accuracy tests described above. The simulation results are shown in Figure 13.

As a final test of the transistor-level transmitter, time-domain baseband I and Q

WLAN signals were generated using Ptolemy. These were read into the transmitter simulation from a dataset, and used to drive the I and Q baseband chains. This simulation required nearly ten hours for 666 symbols. Although this is a long time, the test could be run overnight. The result reveals the output trajectory diagram, power, and whether the spectral mask is satisfied, as shown in Figure 14.



[14]

Summary

Wireless transceiver design requires a lot of simulation techniques and capabilities; often well beyond the capabilities offered by traditional time-domain simulators such as SPICE. The capabilities of frequency-, mixed frequency-, and time-domain simulators have improved greatly in recent years, as shown by simulation data concerning the design described here. For the RF designer of circuits in this field, it may be well worth the effort to try these simulation techniques on the designs.

WD&D

Footnote

1. Tsividis, Y.P., and J.O. Voorman, Integrated Continuous-Time Filters: Principles, Design, and Applications, IEEE Press, 1993.

About the Author

Andy Howard is an applications engineer with Agilent EEsof EDA.

Note:

More information regarding RFDE (Radio Frequency Design Environment, Agilent EEsof simulation and data display tools accessible from within the Cadence Virtuoso Analog Design Environment) and Wireless Test Benches (part of RFDE) may be obtained from: http://eesof.tm.agilent.com/products/ rfde.html *[15] and* http://eesof.tm.agilent.com/docs/rfdedoc2004A/rfdemanuals/rfdewtbsim.html *[16].*

The transmitter design database (including layout) and simulation results discussed in this paper (as well as results not included here) will be available at a later date. Contact Agilent EEsof EDA.

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