COTS 3U and 6U Multiband Receivers

Pentek has developed a cPCI solution with a 3U 16-channel multiband-receiver board and a 6U 32-channel multiband-receiver board featuring 14-bit A/D converters and Virtex-II FPGAs (field programmable gate arrays) for signal processing. Both boards consist of one or two Model 7131 digital receiver PMC modules and a PMC-to-cPCI adapter assembled and tested as a single cPCI board. Both COTS (commercial-off-the-shelf) cPCI boards were designed to maximize configuration flexibility, switching and optimized synchronization for software radio applications such as synchronous data communications, wireless base stations, direction finding, satcom, WLAN, high-frequency sonar and telecommunications.

High density solution delivers four A/D converters, 32 digital receivers and two 3-million gate Xilinx Virtex-II FPGAs in a single cPCI 6U slot.

Flexible Configuration, Switching and Synchronization

The Model 7231 accepts four analog RF inputs at +4 dBm full scale into 50W on front-panel SMA connectors, while the Model 7331 offers two analog inputs. Each input is transformer coupled and digitized by an AD6645 14-bit A/D converter with options for maximum sampling rates of either 80 MHz or 105 MHz. The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, from an external 50 ohm clock source supplied to a front-panel SMA connector or from the front panel LVDS Clock/Sync bus.
A/D converter data is delivered to eight Graychip GC4016 quad multiband digital-receiver chips on the Model 7231 or four quad receiver chips on the 7331. The

maximum input sampling rate for the GC4016 is 100 MHz. Each GC4016 includes four receiver channels capable of independent center frequency tuning from DC to ƒS/2, where ƒS is the sample clock frequency. Additionally, A/D data can be delivered directly to the FPGAs, bypassing the digital receivers for wideband applications.
The front-panel LVDS Clock/Sync bus allows one board to act as a master, driving the sample clock, sync, gating and trigger signals through the LVDS Clock/Sync bus. This supports synchronization of local oscillator phase, frequency switching, decimating filter phase and data collection across multiple boards.
When used with Pentek's Model 9190 clock and sync generator, the boards can support up to 1280 channels, each sharing a common clock and synchronization signals, for very large multi-channel systems including beamforming applications.
The 7231 and 7331 are both equipped with Xilinx Virtex-II FPGAs. Data from the A/D converters and from the GC4016 digital receivers is delivered into the FPGAs, which perform a wide range of user-selectable data packing and formatting functions. Dual port memories inside the FPGAs provide efficient PCI bus transfers by buffering receiver and A/D data.

cPCI Interface

Industry standard 64-bit 66 MHz PLX9656 PCI interface chips ensure full conformance to all PCI bus timing specifications. A PCI bridge connects the two PCI interfaces to the cPCI backplane.

Development Tools for a Variety of Platforms

Pentek's Resources include the GateFlow FPGA Design Kit supporting user-developed FPGA code, GateFlow IP Core Libraries for high-performance FFTs, digital receivers and radar pulse compression algorithms and the GateFlow Factory Installed IP Cores.