Receiver System

Analog Devices introduces a wideband receiver subsystem for cellular base stations that addresses 3G standards, such as CDMA2000, UMTS, and TD-SCDMA. The AD6654 is a mixed-signal device that combines a 14-bit analog-to-digital converter (ADC) with a four- or six-channel digital down-converter (DDC). The AD6654 features a fractional clock multiplier that uses the ADC clock to produce a digital down converter master clock up to 200 MHz. Two 16-bit parallel output ports accommodate high data rate 3G applications. An on-chip interpolating half band can also be used. In addition, each parallel output port has a digital AGC for output data scaling.