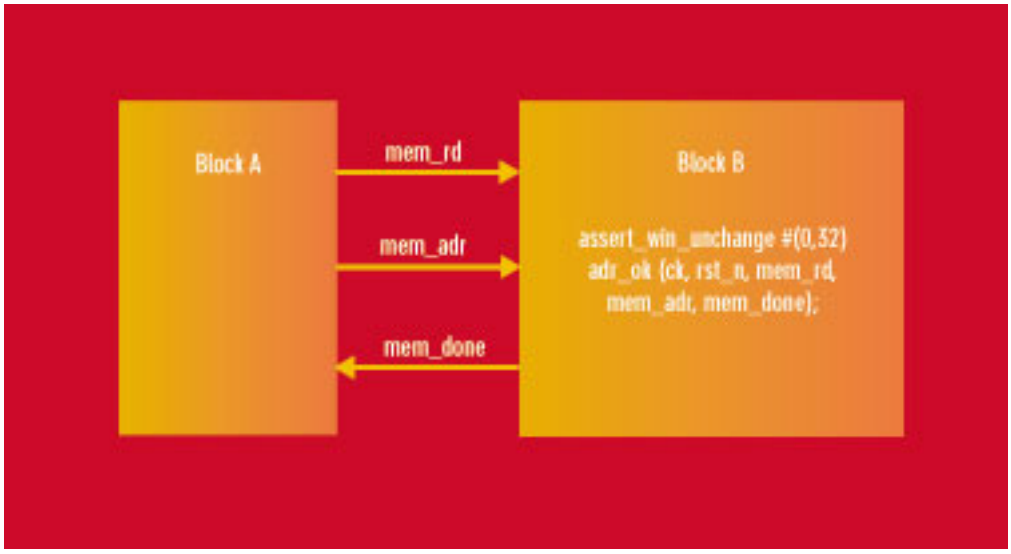
Wireless Chip Design Requires Advanced Verification

By Tony Larson, Verplex Systems Inc.
Consumer demand for more functionality in a wireless device, combined with time-to-market pressures is causing greater challenges for designers. To stay competitive in the Personal Digital Assistant (PDA) market, for instance, companies must be prepared to offer a myriad of wireless applications in addition to supporting the organizational software for which these devices were originally intended. To meet power and size constraints, it is necessary to cram all of these functions onto a single chip.

It is not always possible for one company to possess the expertise to design every function. This is why many wireless companies have adopted a System-On-Chip (SOC) design methodology where specialized blocks of logic called Intellectual Property (IP) are either reused from previous designs or bought from third parties. These logic blocks are then integrated together on a single device.

Using IP saves design time, but may be squandered due to the additional verification time required to verify the complex interactions of these blocks as an integrated system. With verification now consuming close to 70 percent of the design cycle, the use of IP adds to this burden.



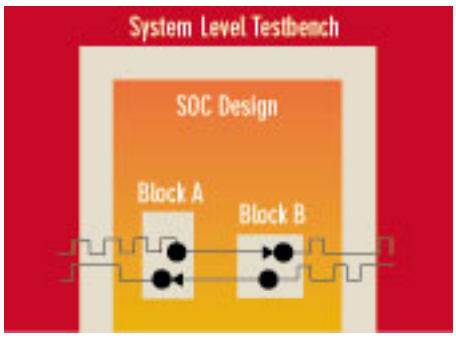
Thorough verification is essential. If an error is detected late in the design cycle, fixing the problem may require the repeating of many design and verification steps, slipping schedules and missing valuable market opportunities. If errors are detected after manufacture, a re-spin may cost a half million dollars or more. If an error is detected in a fielded device, it may cost billions to recall defective devices.

Simulation-based methods have traditionally been used to mimic the many

environmental conditions that a design, or portion of the design, may encounter during normal use. A typical SOC, composed of multiple IP blocks, may require weeks of simulation time. Even more time consuming is the creation of a thorough set of stimuli, or test vectors. When system integrators attempt to verify IP blocks as part of an integrated SOC design, it is not always possible for them to create test vectors to check for every possible interaction that must occur between the blocks to verify that they will operate correctly together.

The verification challenges are even greater when verifying systems that utilize third-party IP blocks, because the intimate design knowledge needed to create interface-level test vectors remains largely with the IP provider. Historically, there has been no automated way to convey this knowledge to the IP integrator. The same is often true for reused IP blocks, since the original designers might be unavailable to help with the integration.

A more thorough verification approach called assertion checking is available which preserves IP design knowledge. Assertions are checks embedded into the design to verify the designer's assumptions about how an IP block should correctly operate, both by itself and in concert with surrounding logic blocks. Assertions help identify errors earlier in the design cycle, where they are easier and less costly to fix.



Assertion checks may range in complexity from simple mutual exclusivity checks (checking that two signals do not have the same value simultaneously) to more complex, sequential signal interactions such as handshaking (checking that a block always responds appropriately and in a timely manner when a signal is sent from another). Once assertions are embedded into a design, assumptions the designer made about how the block should operate as part of a system are verified wherever and whenever the block is used.

One hindrance to utilizing assertions has been the lack of a common method of specifying them. The Open Verification Library (OVL) initiative (http://www.VerificationLib.org) changes that and is used today by designers, verification engineers, IP providers and integrators. OVL consists of an open-source, Verilog hardware description language (HDL)-based library of assertions as a means for capturing design knowledge, which then becomes portable with IP blocks wherever they are integrated.

Several design automation tools are now supporting OVL including simulation-based tools and formal verification tools. The thoroughness of OVL checks can be boosted when used with formal verification tools. Formal verification, unlike simulation-based verification, requires no test vector stimuli. It uses mathematical techniques

to exhaustively determine whether it is possible to violate an assertion. If possible, tools automatically generate an example test vector to demonstrate the violation.

Creating modern wireless devices with diverse functionality and within a short market window often requires an aggressive SOC methodology with inherent IP verification complications. OVL assertion checks are a concise means of capturing IP design knowledge, automating integration, and hastening verification by uncovering more bugs earlier. Formal verification can further increase the thoroughness of OVL assertion checks, reducing schedule slips, re-spins or recalls due to missed design errors.

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