Clock Dividers

Six high-speed, LVPECL and LVDS programmable clock dividers have been released from Micrel's Precision Edge Timing & Distribution family. The SY89871/2/3/4/5/6 are precision 2.5 V & 3.3 V high speed LVPECL and LVDS programmable clock dividers with an input stage that includes internal termination and the ability to accept any differential input source. Whether the input signal is AC-coupled or DC-coupled, no external components are required in the signal path to interface to the SY89871 family. The SY89871 family of non-PLL clock dividers is optimized for applications which require low jitter and skew performance. Within-device skew is less than 15 ps; rise and fall times are less than 250 ps. Designed to accept a high frequency (e.g. 622MHz or higher) CML, LVPECL, LVDS or HSTL clock input signal, this family divides down the frequency with programmable divider ratios of 1, 2, 4, 8 or 16 to create a phase-aligned, clock subset of the input clock. The SY89871 family is offered in a small (3 &#215 3 mm) 16-pin MLF package and guaranteed over the &#150 40&#176C to +85&#176C industrial temperature range.
www.micrel.com; (510) 476-5963