Phase Lock Loops

National Semiconductor introduces a new family of PLLatinum&#153 phase lock loops (PLLs) for cellular applications. This family of delta-sigma fractional-N PLLs uses digital modulation techniques for excellent phase noise, spurs and lock time performance in applications requiring fine frequency resolution. The first in the family, LMX2470, is housed in a 3.5 &#215 4.5 &#215 0.6 mm thin chip scale package that is ideal for use in 2G, 2.5G, and 3G mobile handsets, base stations, WLANs, and other wireless communications systems. The device features a maximum RF operating frequency of 2.6 GHz and an 800 MHz IF frequency. The device allows users to software select the modulator order. It is optimized for low power consumption, with 4.1 mA total current at a 2.5 volt supply voltage.