Electrical Performance of Microvia PCB Materials

Substrates based on FR4 core constructions utilizing low loss microvia dielectrics can offer low cost, high performance.

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High density module substrate and PCB requirements are driving the need for high density interconnect (HDI) design capabilities using laser microvias (note that &quotHDI&quot, &quothigh density&quot, and &quotmicrovia&quot are often used synonymously when describing these types of designs). Many of these applications require both RF and digital circuitry on the same HDI, multi-layer circuit board or module. The advantages of HDI designs include lower layer counts, smaller PCBs, lower costs, improved electrical performance, thinner constructions, and lighter weight end products. An additional benefit for PCBs using HDI outer layers is the ability to incorporate high density area array packages to further increase the performance of your base station, wireless PDA/phone or WLAN design.

WLAN has been one of the true bright spots in the recent economic downturn. Global demand for WLAN shipments had been projected at 15M units in 2002 growing to 45M in 2005. However, recent numbers have shown that actual 2002 shipments were closer to 25M, more than doubling the number of units sold in 2001, and some are now projecting 2005 shipments to surpass 100M units. Clearly, with current economic conditions, there are not many market segments that are showing sustained growth rates of 50 - 100% like WLAN.

One of the greatest factors affecting the adoption rate of new technologies such as WLAN and Bluetooth is acceptable pricing. At the same time, higher bandwidth and lower power consumption require improved electrical performance while needs for smaller product sizes present additional constraints upon circuit designers and substrate manufacturers. A typical WLAN card is shown in Figure 1.

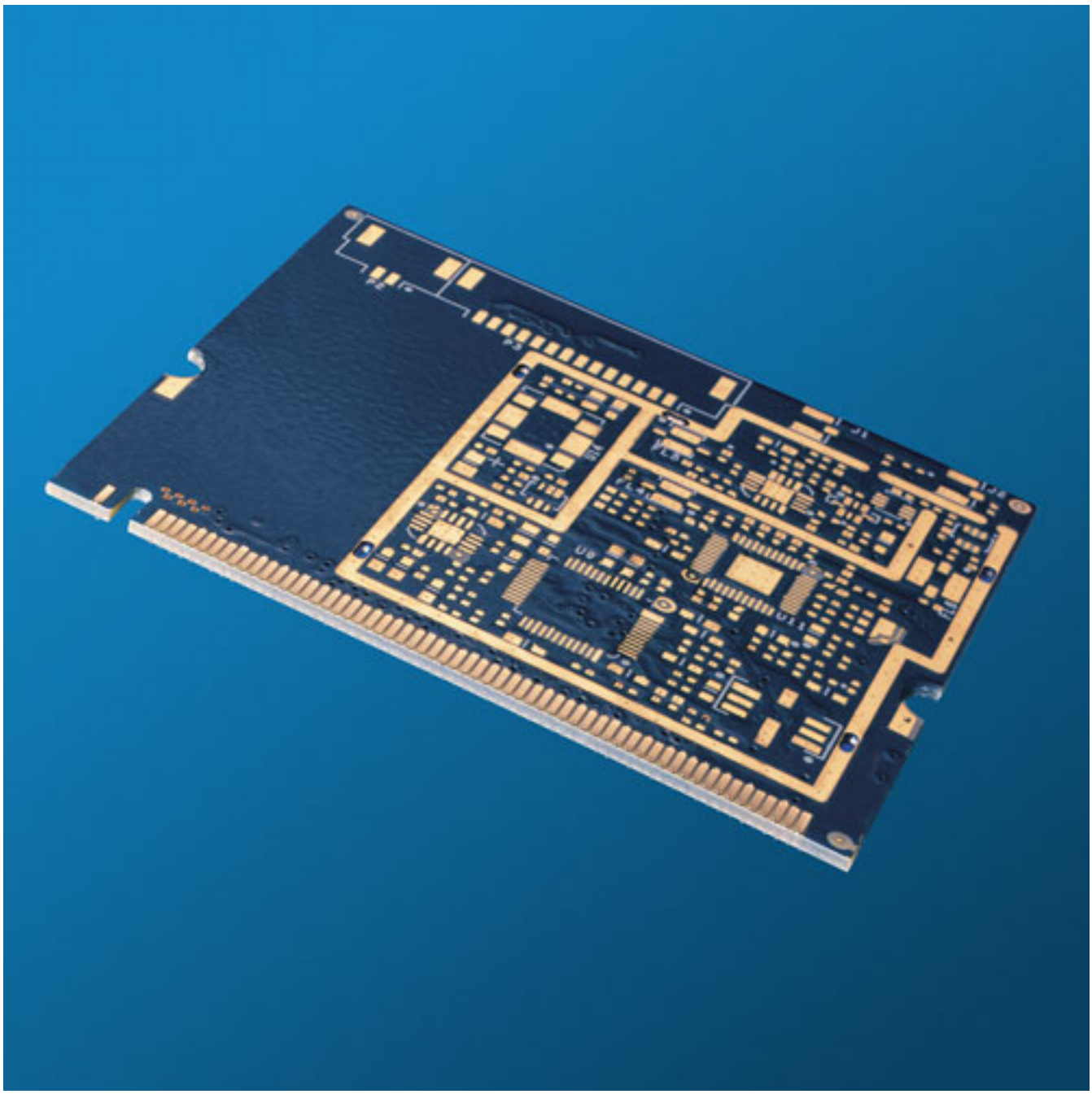

Figure 1. Commercial WLAN card operating at 2.4 and/or 5.2 GHz.

Electrical Performance Challenges

Increased bandwidth and operating frequencies will continue to drive needs for increased signal integrity which in turn places added value on the electrical performance of PCB and substrate materials. Controlled impedance designs require improved thickness uniformity, minimal variation of dielectric constant and loss over the operating frequency range, and thinner dielectrics due to reduced trace widths in high-density applications.

Total signal losses are comprised of losses due to both the copper conductor and the dielectric. However, as frequencies increase above 1 GHz, such as in many WLAN and RF module applications, dielectric losses begin to dominate. Many designers find that signal losses often become more significant with the move from

2.4 to 5.2 GHz designs. Therefore, designing with a low loss dielectric can minimize the total loss of a given design.
A low Dk material enables the use of wider traces for the same impedance, maximizing conductor as well as dielectric losses. Low loss and low DK materials provide superior signal integrity for digital signals over a given length of circuitry and minimize power losses for RF applications.

High-Volume manufacturing Challenges

Microvia PCBs and substrates are manufactured in large panel, usually 457 mm times> 610 mm (180 times> 240) or larger, format using laser processing, predominantly CO and YAG. Some of the critical characteristics of HDI dielectrics that facilitate low cost, high-volume production include laser via drilling speed, homogeneity of the material, and lamination cycle. Some of these material attributes, as well as electrical performance values, are shown for common PCB materials in Table 1.
Laser drilling speed is a function of the dielectric material composition. Organic materials (epoxy, BT, and PTFE resins for example) laser drill significantly faster than glass based materials. Faster laser drilling throughput can translate directly into cost savings by increasing the capacity of the current laser drills at a given fabricator and reducing operating expenses.
The relative homogeneity (glass weave, ablative match of resin and reinforcement, etc.) of the material will also be important in establishing microvia hole quality and the variability of the laser drilling process. For example, five laser pulses may be enough to ablate through a resin rich area of FR4, yet may not ablate through a glass rich area (a knuckle), leaving an open.
For all applications using HDI dielectrics, material-process interactions such as via taper angle, wicking, and dielectric cracking can all affect the density capability of a fabricator. Nan Ya engineers presented a useful, detailed analysis of these and other via quality issues, quot>7 Items of Laser Drilling Quality,quot> during a recent Taiwan Printed Circuits Association (TPCA) meeting.

Test Board Stack-up and Processing

As seen previously in Table 1, there are many material choices for these types of boards. However, only the three most cost effective options were chosen for further evaluation in this study. Four layer (1/2/1) and six layer (1/4/1) (notation meaning microvia/core/microvia layers from top to bottom) boards were manufactured with different materials. All versions used a FR-4 core with buried and laser blind vias. Resin coated copper foil (often called RCF or RCCreg>), FR4 prepreg or MICROLAMreg> 630 dielectric layers were laminated on each side of the core as shown in Figure 2.
The picture in Figure 2 shows the woven glass FR4 core. The expanded PTFE (ePTFE) micro-reinforcement makes the MICROLAM 630 (layer 1-2) appear white while the dark areas are resin rich, where BT resin flowed during lamination.

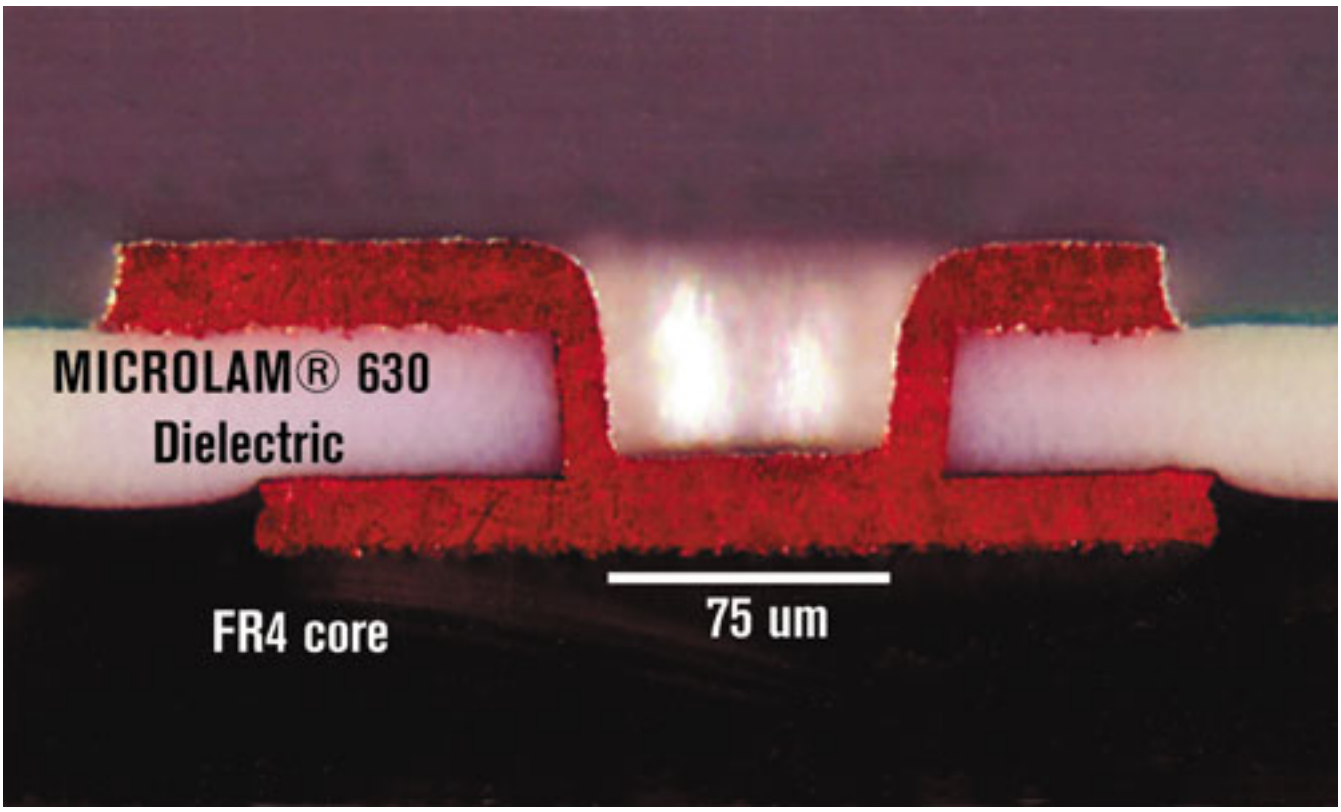

Figure 2. Cross-section showing MICROLAM 630 dielectric on an FR4 core (note the 75 um microvia, the dielectric is 57 um thick).

RF Test Methodology and Transmission Line Measurements

Test boards were fabricated to evaluate the relative electrical performance of the three dielectric materials (RCC, MICROLAM 630, and FR4) using microstrip transmission lines. Measurements of insertion loss for RF applications were done using an Agilent 8720E network analyzer over a frequency range of 50 MHz to 10 GHz.

Testing was done using edge launch PCB connectors. Microstrip lines of 25 and 200 mm in length were both tested, thus allowing connector effects to be quantified. The S21 data was obtained by using a Cascade Matrix test method developed at W.L. Gore. The method is similar to a network analyzer TRL calibration. The Cascade Matrix method assumes repeatable connections, requires two samples of different lengths for the same test condition, and more accurately accounts for connector losses than the commonly used quot>stored trace dividequot> method. The Cascade Matrix Method is performed as follows:

1. The uncorrected scattering parameters of a short and long sample of the same material are measured.
2. The S-parameter matrix is converted to a Cascade matrix.
3. Using linear algebra the propagation constant is extracted.
4. S21 for the long sample minus connector effects is charted.

Figure 3 shows the measured insertion loss as a function of frequency for four different options. The 86 um thick MICROLAM 630 and 125 um FR4 both used 210 um wide traces which reduced copper losses. The difference between these two shows the effect of lower dielectric losses. The 57 um MICROLAM 630 and 75 um thick RCC used 125 um wide traces and their relative performance can also be

seen. The larger cross-sectional area of a wide trace reduces copper losses due to the skin effect at gigahertz frequencies. Note that in order to increase the trace width, the thickness of the dielectric also had to increase in order to maintain an impedance of 50 Ohms.

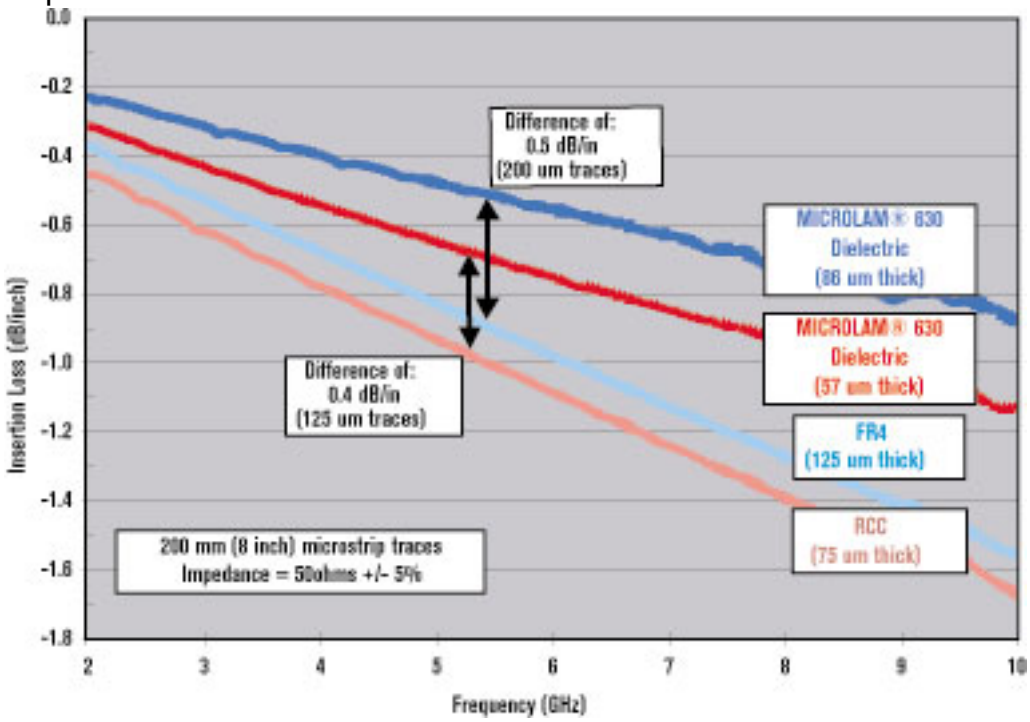

Figure 3. Insertion loss for 200 mm long, 50 Ohm microstrip traces (125 mm wide traces for 75 mm RCC and 57 mm thick ML630, 210 mm wide traces for 125 mm FR4 and 86 mgr>m thick ML630).

Conclusions

A substrate material with superior electrical properties at gigahertz frequencies can significantly improve RF signal transmission as well as RF filter performance. The dielectric loss factors specified by the suppliers of resin coated epoxy foil, FR4, and MICROLAM 630 dielectrics seem to fit well with the measurements made.
At RF frequencies, measurements show that transmission losses are strongly effected by both copper and dielectric losses. Using a low Dk dielectric enables the use of wider traces while maintaining a thin layer 1-2 thickness that helps to keep an acceptable microvia aspect ratio (thickness/width > 1). Wider traces along with low loss dielectrics will minimize both conductor and dielectric losses for improved electrical performance.
The use of low loss microvia dielectrics may allow RF and digital circuit designers greater design freedom due to reduced total signal losses. This in turn enables the designer to maximize system performance (greater wireless range and/or data rate) or use some of their loss budget elsewhere in the system design. These losses can benefit both transmit and receive portions of a design. Lower losses will also reduce power consumption, providing:

1. Longer battery life
2. Reduced thermal requirements
3. Reduced EMI

Lower PCB losses can provide the ability to have longer distances between components on a substrate or PCB, thus allowing greater freedom during layout.

Other options that reduced PCB losses may provide include using lower performance components or using PCB traces as the RF antenna, instead of using a separate cable antenna. These options can reduce the number and/or cost of components and minimize the total system bill of materials (BOM), providing cost/performance solutions for RF designs.

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t1>I>Editor's Note: Portions of this paper, along with buried passive RF filter test results, were presented at the March 2003 IPC Printed Circuit Expo in Long Beach. For a list of references that accompanies this article, please email kpotts@reedbusiness.com./I>/t1>

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