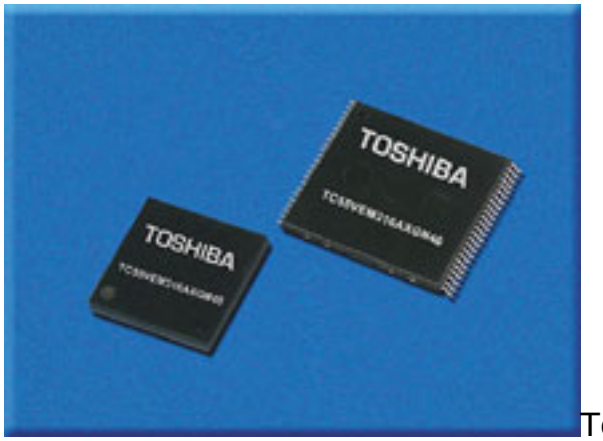
Low Power SRAMs



Toshiba America Electronic Components (TAEC) with its parent company, Toshiba Corporation (Toshiba) announced a new family of full-CMOS 8 megabit (Mb) Static Random Access Memory (SRAM) devices. These eight new low-power devices were designed utilizing 0.15 micron (m) CMOS technology to meet the specific design requirements of the dynamic wireless market, including reduced power consumption, faster access and cycle times, and packaging flexibility.

Select devices in this new family can achieve an access time of 40 ns at voltages ranging between 2.7 V - 3.6 V. Faster access times such as those achieved by these devices significantly reduce memory system wait time in wireless applications such as cellular phones.

For designers who require high speeds but are more concerned with low power consumption, Toshiba's new family of devices can achieve access times of 55 ns to 85 ns at voltages ranging between 1.65 V and 3.6 V. In addition, each product within this new family incorporates an internal voltage down converter, enabling the devices to support wider voltage levels long-term. Three packaging options are available within this family of devices, providing additional design flexibility.

In addition to the existing 48-pin Thin Small Outline Package (TSOP) Type-1 measuring 12 mm &#215 20 mm used to house Toshiba's previously-released 8Mb SRAMs, Toshiba has added two smaller packages including a 48-pin TSOP Type-1 measuring 12 mm &#215 14 mm, and a space-saving 48-pin Fine Pitch Ball Grid Array (FBGA) package measuring 7 mm &#215 7 mm. All packages offered are lead-free.

Source URL (retrieved on *07/23/2014 - 2:57am*):
http://www.wirelessdesignmag.com/product-releases/2002/02/low-power-srams?qt-most_popular=0