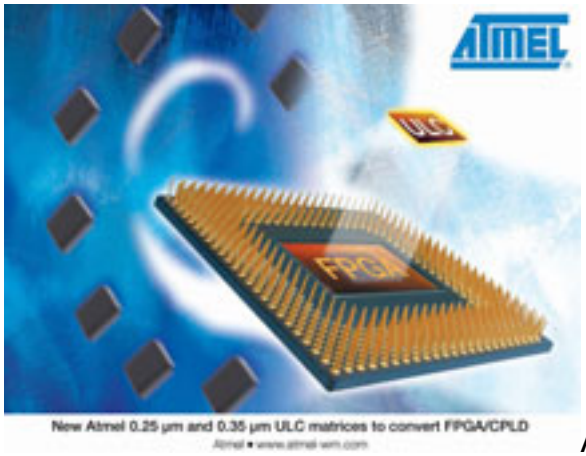
Embedded Memory Blocks



New Atmel 0.25 µm and 0.35 µm ULC matrices to convert FPGA/CPLD

Atmel&reg Corporation announced a complete set of new 0.35 &#956m and 0.25 &#956m matrices to convert most FPGA/CPLDs to Atmel's Ultimate Logic Conversion (ULCs), enabling significant cost savings for system makers.

With these 0.35 &#956m matrices, Atmel can handle up to 400 Kbits Dual Port RAM and 780K gates in a single chip. These memory blocks are 100% compatible with embedded memory blocks from popular FPGA/CPLD makers Xilinx and Altera. Both Synchronous and Asynchronous DPRAM are supported. Each port parameter can be individually configured. ULC configuration uses customization levels in order to offer very low NRE charges.

By removing the silicon area needed for programmability and implementing the memory in ULC memory blocks, Atmel can significantly reduce the size of the die and can bring cost savings up to 80% for large FPGAs. Using the 0.35 &#956m process an FPGA with 98 K bits DPRAM and 200K logic gates is approximately 252 mm. The equivalent ULC is only 104 mm^2.

With its 0.25 &#956m process Atmel ULCs can support up to 1500 Kbits DPRAM and 1800K ASIC gates which is equivalent to 7000K FPGA gates.

The ULC's internal frequency can be run at a much faster speed than that of conventional FPGAs. By inserting standby periods, power consumption can be typically 90% lower than its FPGA counterpart.