Package

STMicroelectronics has introduced its latest generation of chip-scale package for power integrated circuits as well as six N-channel MOSFETs that take advantage of the new package to slash size and weight while boosting thermal and electrical performance.

The PowerFLAT case, available in 6 &#215 5 mm and 5 &#215 5 mm outlines, adopts a micro-lead-frame design that, partly by replacing leads with terminal pads, ushers in nothing less than an entirely new chip-packaging concept. Power devices ensconced in the PowerFLAT package will find wide acceptance in DC-DC converters and the battery management sections of portable equipment.

Of the two outlines unveiled, the 6 &#215 5 mm PowerFLAT case is pin compatible with a standard SO-8 package, yet accommodates 118% more die area. Moreover, both outlines feature an exposed back slug that connects the MOSFET die to the printed circuit board for superior heat dissipation. The maximum height of the PowerFLAT is just 1mm. In addition to its light weight and small size, the PowerFLAT package reduces parasitic inductance to yield better MOSFET performance.

Riding the roll out of the PowerFLAT packages are six N-channel MOSFETs boasting high efficiency and solid performance. Offered in the 5 &#215 5 mm outline version are the STL22NF10, with a 100 V drain-source breakdown voltage (BV_{DSS}), 65 mOhm typical on resistance ($R_{DS(on)}$), and 22 A continuous drain current (I_D); the STL28NF3LL, with a $V_{(BR)DSS}$ of 30 V, a typical $R_{DC(on)}$ of 5.5 mOhm, and an I_D of 28 A; and the STL4NM60, with a 600 V BV_{DSS}, 1.5 Ohm $R_{DS(on)}$ (typical), and 4 A I_D.

The remaining family members harnessing the 6 &#215 5 mm case comprise the STL30NF3LL, with a BV_{DSS} of 30 V, a typical $R_{DS(on)}$ of 6 mOhm, and an I_D of 30 A; the STL35NF10, with a 100 V BV_{DSS}, 25 mOhm typical $R_{DS(on)}$, and 35 A I_D; and the STL35NF3LL, with a 30 V BV_{DSS}, 6 mOhm typical $R_{DS(on)}$, and 35 A I_D.

All six new PowerFLAT MOSFETs use ST's unique second-generation STripFET technology, which yields transistors having a very low on-resistance and minimal gate charge. As a result, devices show a dynamic performance that is superior to the closest competition. In addition, the STL4NM60 plies a revolutionary MOSFET technology called Mdmesh&#153 that combines a multiple-drain process with ST's horizontal layout. The benefit to the design is a very low on resistance, very high dV/dt and impressive avalanche characteristics.