Software Teams with a Logic Analyzer or New Measurement Technique

By designing in a connector, performance can be rapidly evaluated, thereby supplanting the cumbersome, time-consuming oscilloscope connections of the past.

By Ed McGettigan, Xilinx and Art Porter, Agilent Technologies
One of the clear trends in bus systems is the move from system-synchronous buses to source-synchronous buses. In source-synchronous systems the clock and data move together throughout a system, with the clock becoming an intrinsic part of the data. In addition, over the past eighteen months a variety of high-bandwidth, source-synchronous differential signaling buses have emerged. The most popular ones are RapidIO&#153, Hyper Transport&#153 and SPI4 Phase II (SONET Packet Interface). It is very difficult to debug interconnections in such systems. They operate so very fast, at data rates on the order of 800 Mb/s-per channel, and with 16-channels there are huge amounts of data in transit.
With system complexity growing as just described, the higher bus speeds create tighter margins in both time and voltage. So there is more likelihood for things to go wrong. And there are still the all-too-familiar hindrances of trying to reach a node with a conventional oscilloscope probe. How is someone going to confirm signal integrity in systems which may have tens of buses with tens of signals on them and thousands of operating conditions? There simply isn't time to make all these measurements with a traditional oscilloscope.
But a new validation technique called eye scan offers a solution. It came into being with a software feature that Agilent has introduced as an adjunct to the existing 16760A Logic Analyzer. Eye scan enables the user to monitor all arriving signals on all buses at once for activity, in a time range centered on the clock and over the full voltage range of the various signals. The signals are then displayed as an image that is similar to the familiar eye diagram (Figure 1).

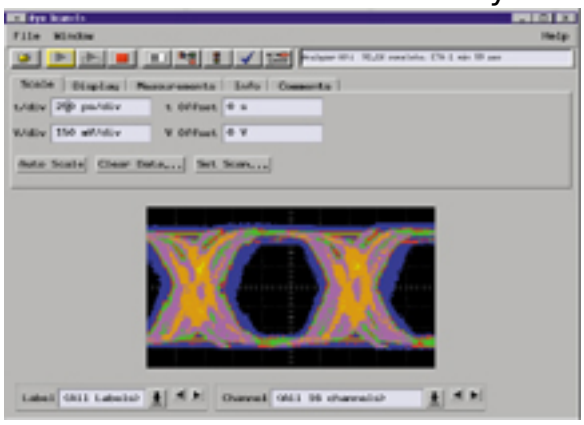

Figure 1. The Eye Scan Image

The eye scan feature of the Agilent 16760A Logic Analyzer is supported by several types of probes. The most important probe employs a Samtec 100-pin connector for interconnecting the Logic Analyzer to the device under test. The user designs the Samtec connector into the circuit board connected to the desired nodes of a bus. Once the connector is designed in, hooking up the 16760A through the mating connector takes seconds. It is thereby making up to 16 differential connections simultaneously.
In actuality, eye scan provides five measurement tools:
&#149**Cursors** - Two manually-positioned cursors enable the user to accurately read the time and voltage coordinates of the trace appearing in the scan, as shown in Figure 1.
&#149**Eye limit tool** - The eye limit tool is a single-point cursor that can also be positioned manually. The readout indicates the inner eye limits detected at the time and voltage coordinates of the cursor.
&#149**Histogram Tool** - The histogram tool displays the relative number of transitions along a selected line. The time range and voltage levels of the histogram are selected by manually positioning a pair of cursors. The cursors denote the voltage level as well as the beginning and end times of the histogram.
&#149**Slope tool** - The slope tool indicates the slope (dV/dt) of a segment established by two manually-positioned end points.
&#149**Polygon tools** - 4-point and 6-point polygon tools are provided. These let the user to create a 4-point or 6-point polygon mask on the display for visual comparison with the eye opening.

Eye scan enables the user to set a number of variables. These include the number of clock cycles to be evaluated in each time and voltage region as well as the time offset, volts/division and voltage offset &#151 also the time resolution of measurement and the voltage resolution of measurement.
Results can be displayed for each individual channel &#151 or the channels can be overlaid. In addition, the eye scan data can be stored and recalled for later comparison or analysis.

How Eye Scan Works

Eye scan enables the user to perform eye analysis across multiple channels of virtually any number of parallel buses. It scans over time and then over voltage. When the user hooks up eye scan and presses 'Run' the logic analyzer begins storing in its memory the information to be later viewed on the screen.
To acquire the information for an eye scan it samples at one time/voltage coordinate region (or pixel) for a specified time to determine if the signals transits the pixel region. Another way of saying this is that the user is examining a very small time/voltage box to see if the signal ever passes through that region. At the extremes, if the signal always intersects the window, it is painted white. If it never intersects the window, the counter registers zero and the region will be displayed as black. The percentage of time it transits can be perceived as a color or a gray shade and also can be displayed by using the histogram tool.
The time width (T_{min} to T_{max}) in the horizontal direction can be from 4 ns before the clock to 4 ns after, as shown in Figure 2.

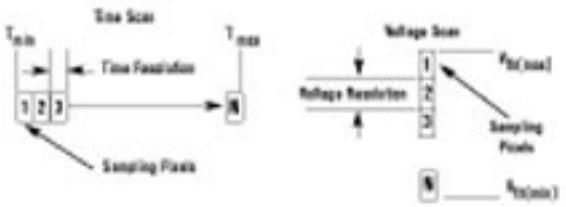

Figure 2. How Eye Scan Constructs the Image

If time resolution is reduced so that the samples in effect, taking thinner and thinner slices it thereby shrinks the size of the pixel, and therefore takes longer to scan. Once the count has been completed at a given pixel, eye scan moves on to the right and looks at the next slice of time. The clock, which is not shown is actually at center screen, assuming the time offset is set to zero. The same process occurs along the vertical axis, incrementing the threshold voltage (V_{TH}) vertically and moving in increments as small as 10 millivolts &#151 as governed by the voltage resolution that has been programmed. This is performed in the same way as the time scan for each voltage increment until eye scan has run through the range that has been selected on the screen.

By paging through 'Pod A1 Channel 0' the user can view the waveform on all the channels. There is also the option of viewing a composite image enabling the user to view all channels at once. In the composite mode, individual channels may be highlighted to identify offending signals quickly.

As a measurement instrument, eye scan delivers an equivalent bandwidth of approximately 2.3 GHz. Threshold accuracy at &#177 1% (+30 mV) and time base accuracy at &#177 50 ps is not quite as good as one would expect from a scope but certainly ample for validating performance in virtually any application. Jitter is 12 ps rms; the noise floor is 25 mV p-p.

For the designer that wants to see how performance might be altered if a value changes, a parameter, such as voltage, in one or more circuits can be varied to see if this affects the waveform in any way. If a problem occurs, the designer may then decide to use a conventional oscilloscope to look at certain waveforms in more detail. Thus the user can concentrate on those situations in which an event fails to occur, thereby concentrating on just the bad 'corner' cases.

An Example

Xilinx is putting eye scan to work evaluating signal performance of high-bandwidth, differential signaling buses with 16 channels using our new Virtex&#153-II Platform FPGAs. This is our latest generation field programmable gate array (FPGA) that supports up to 8 million system gates. It provides up to 3 million bits of RAM and twelve digital clock managers that support removing of clock delays, dynamic phase shifting and clock frequency synthesis. The Virtex-II Platform FPGA has been designed to work with high-speed differential signaling buses &#151 such as RapidI/O, HyperTransport&#153 and SPI4 Phase II.

The board, shown in Figure 3, with the Samtec 100-pin connector designed in, supports five different variations of differential signal standards. Agilent's eye scan is used to analyze three different paths including one that comprises 15 inches of PCB trace that loops from the transmit interface of the FPGA back to the receive interface of the FPGA. The eye scan equipped 16760A Agilent Logic Analyzer is connected to the Samtec connector at the bottom, just to the right of the display at the bottom of the board assembly in Figure 3.

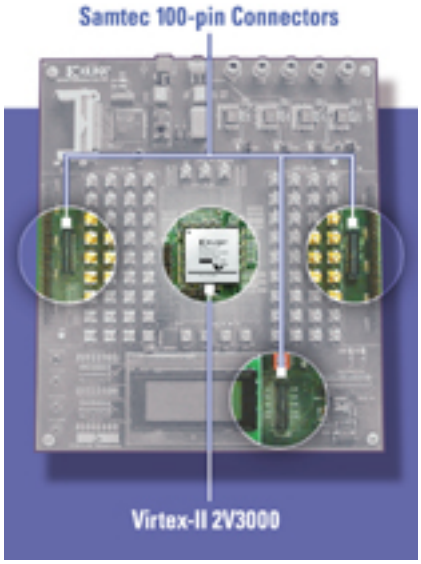

Figure 3. Xilinx's Virtex II FPGA Evaluation Board

This board enables Xilinx designers to test any high-speed differential signal bus &#151 as well as interoperability between a variety of different sources using the SMA connectors. One of the really significant features is the fact that eye scan is able to analyze up to 16 channels of the bus in parallel. It scans through all of the voltage and time areas so as to deliver a graph similar to the one in Figure 1 for the entire bus. The scanning time depends upon the granularity programmed for the image and the transitions of the signal. In the case of this Xilinx board, scanning all 16 channels required approximately 5 minutes.

If this technology was not available, designers would have to individually probe and check each channel of all the buses. Eye scan is the only measurement technique that Xilinx has been able to identify that can gather eye diagrams from more than a few channels at one time.

Once scanned, designers can then review all the eye scans, at their leisure, to gain a clear picture of the full dynamics occurring on all channels of the bus. They can view the behavior of any channel by simply clicking on the paging buttons shown adjacent to &quotPod A1 Channel&quot shown in Figure 1.

When viewed overall, eye scan bolsters the confidence in reliability by providing the user with a vast amount of data because it stores what are in effect millions of eye scans. It should be clear that eye scan is an adjunct to an oscilloscope, not a replacement or a substitute. But what distinguishes eye scan can best be described as easy and complete access.

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