

Low Current Advantages of CMOS Technologies for RFIC Designs

CMOS is increasingly capturing the GHz frequency space as the RF technology of choice.

By David Burnell, Mark Cavin, Craig Frost, and Eric Naviasky, Tality Corporation
The time for broader adoption of straight CMOS radio frequency integrated circuits (RFIC) for mobile devices has arrived. Historically, RFIC designers have turned to relatively expensive processes such as Silicon BiCMOS (CMOS with a high performance bipolar NPN transistor), Silicon Germanium (SiGe) BiCMOS and Gallium Arsenide (GaAs) for RFIC designs. At today's feature sizes and levels of integration, CMOS is increasingly capturing the GHz frequency space as the RF technology of choice.

While BiCMOS and GaAs solutions provide the performance enhancements needed for high frequency RF designs, they do so at a cost premium. GaAs is the most expensive of these technologies, and therefore only used at the highest frequencies where BiCMOS is not adequate. BiCMOS requires additional lithography and processing steps over its straight CMOS counterpart, while GaAs is a more complex technology whose (significant) development lags the massive investment of mainstream CMOS. Larger CMOS wafer sizes, denser design rules, more levels of metal interconnect, and huge economies of scale make CMOS the low-cost leader whenever its performance is sufficient to meet the design requirements. These cost advantages will only increase as foundries move to twelve-inch wafers in the .13 um technologies this year. Add to this RF/Mixed Mode CMOS technologies in the major foundries have added desirable passive components like inductors, MIM caps and varactors and the only question is, "what is the performance limit of CMOS technology?"

The answer to that question is fluid. Today's advances in CMOS RFIC design make the technology a suitable and attractive alternative for Bluetooth-enabled devices and other portable applications. Through novel design techniques and circuit architectures pagers, cordless phones, GPS receivers, and other wireless devices can be designed to meet talk time and battery drain requirements. Lower operating voltages and off current reduce the ultimate RFIC current draw leading to increased battery/product life. This presents another cost advantage - this time to the end user.

Historic Limits of CMOS in the Wireless Environment

Before outlining the strengths of CMOS for wireless devices, let's start by reviewing the disadvantages of CMOS compared to BiCMOS that have precluded the use of CMOS technology in the past. These are lower ratio of transconductance (g_m) to drain current (I_d), higher noise, and lower breakdown voltages.

At similar feature sizes, CMOS requires more current to obtain the same level

Low Current Advantages of CMOS Technologies for RFIC Designs

Published on Wireless Design & Development (<http://www.wirelessdesignmag.com>)

of gain. Available on-chip inductors are small with relatively low Q. These factors typically result in higher power budgets than required for bipolar processes. The inherent excess and higher noise factors get worse as designs go deeper into submicron territory for CMOS RFICs.

The lower breakdown voltages of CMOS RFICs as compared with bipolar processes translates to lower operating (rail) voltages which tend to limit the dynamic range of CMOS RFICs.

While significant, these historical drawbacks are no longer the defining factors in selecting the most competitive RF technology. Given the state of today's CMOS technology and projected trends, the strengths are outshining the shortcomings and enabling design alternatives that circumvent past drawbacks. In addition to reduced costs, come the collateral benefits of shorter delivery times and production cycles, and finer lithography/feature size for optimizing RFIC design and performance, and most importantly higher levels of integration with digital circuit blocks. This article will focus on the application of CMOS to low current RFIC designs, in particular highly integrated RF transceivers.

For mixed signal system on chip (SOC) applications, bipolar processes simply don't handle digital signal processing as well as CMOS. The feature size reduction of pure CMOS processes has led to advances in RFICs. Mixed signal chips operating up to 2.5 GHz have become a commercial reality in recent years. By using the same process for traditional digital or baseband circuitry as the higher frequency RF circuitry, chips can be merged that otherwise would be divided into multi-chip sets. Besides cost advantages, single chip integration reduces current-draw by reducing the number of bondpads and offchip loads that are necessary to drive multiple, non-integrated chipsets.

RF/Mixed Mode CMOS processes in today's foundries offer the integration of resistors, capacitors, and inductors further reducing the number of off-chip drivers. Since the integrated capacitors and resistors can vary 20 percent or more, the advanced analog circuits require calibration or trimming. CMOS logic can do this without external intervention using sophisticated automatic calibration algorithms that are readily implemented.

Smarter power management blocks are possible with CMOS. By using CMOS, designers can use sophisticated digital blocks to calibrate or control custom analog blocks. The CMOS controller can lower supply currents by adjusting biasing of power hungry analog blocks when not in use. Low Noise Amplifiers (LNA) and Power Amplifiers (PA) can be biased at reduced current levels when amplifying smaller signals. Circuits can be duty cycled through sleep- and wake-up sequences controlled by digital timers customized for a given application. The extra digital complexity is well worth the current (power) savings in many applications, with negligible impact on chip size and yield.

Low Current Advantages of CMOS Technologies for RFIC Designs

Published on Wireless Design & Development (<http://www.wirelessdesignmag.com>)

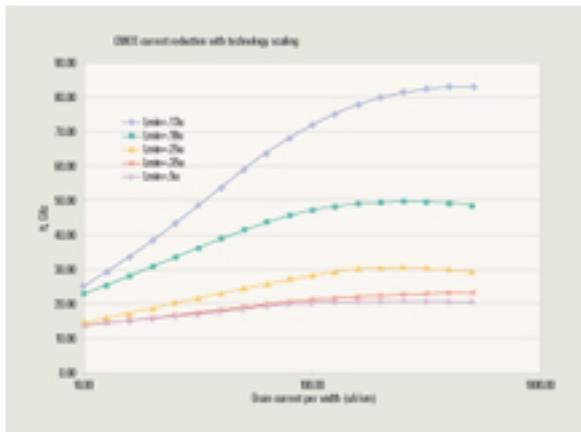


Figure 1. f curves

Short channel dimension makes CMOS more effective for RF. The disadvantage of low Gm substantially erodes as CMOS feature sizes approach .13 um and below. CMOS ft or unity current gain frequency (which is proportional to Gm) becomes quite respectable at reasonable current densities for deep submicron environments (See Figure 1). With these improved ft's, many RF CMOS circuits become "current" competitive with their Bipolar or BiCMOS counterparts. Figure 1 shows some advances made in ft as CMOS processes have advanced. The inherent low parasitic capacitances of deep sub micron CMOS further improve the performance of traditional circuit topologies when implemented in CMOS. RF building blocks designed in .25 u or .18 u processes such as LNAs and Image Reject Mixers (IRM) are feasible.

A good example of using CMOS to lower current in an RFIC design is found in fractional-N modulated frequency synthesizers. Rather than upconvert baseband or IF signals using an RF mixer or quadrature modulator, the synthesizer divider (already required for local oscillator generation) is modulated or dithered between two or more divide values. The VCO in conjunction with a PA and this synthesizer form the RF Transmitter. Although delta sigma modulators can be complex circuits, they are gaining popularity because they typically draw less current than mixers operating at RF frequencies. Other prior issues such a quantization noise and linearity of VCOs can be readily addressed through CMOS designs of low frequency filtering and calibration circuitry.

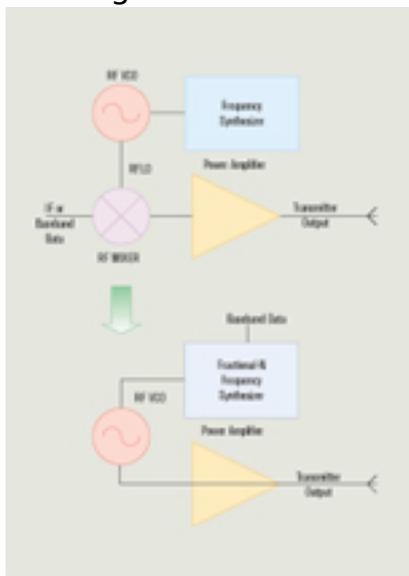


Figure 2. Transmitter Architectures

It is also important to note that as the CMOS geometries shrink, the supply voltage decreases and levels of integration mushroom, digital signal processing becomes competitive with analog implementations. Functions such as demodulation and filtering are therefore well suited for digital signal processing.

The nearly ideal CMOS switch. Another advantage to using CMOS in RF as well as lower frequency applications is the availability of nearly ideal switches. These switches are used to tune conventional circuits by switching in and out resistors, capacitors, inductors, or active devices. In addition, certain circuit topologies such as switched capacitor filtering are only realizable with the nearly ideal switches available in CMOS. Because CMOS designs allow the implementation of excellent switches, switched-capacitor sampled-time design techniques can provide another degree of freedom in power/performance tradeoffs.

Making the most of CMOS device physics. Several other characteristics of CMOS devices are useful in RF design. These include: complementary designs that take advantage of the high performance p- and n-channel devices, use of folded topologies to allow operations at reduced supply voltage, sub-threshold device operation for bipolar-like characteristics, and fast operation even at low drain voltages which facilitates rail-to-rail signal swings.

In summary, as with any technology the key to success lies in exploiting its strengths and merits while mitigating inherent disadvantages. Through careful design techniques, process modeling and wafer fabrication, sub-quarter micron CMOS technologies are quickly becoming processes of choice for RFIC designs up to and including the 2.4 GHz ISM band. And the march of CMOS technology up the frequency spectrum shows no sign of slowing down.

David Burnell (dburnell@tality.com), Mark Cavin David Burnell (dburnell@tality.com), Mark Cavin (mcavin@tality.com), Craig Frost (craigf@tality.com), and Eric Naviasky (enav@tality.com) are with Tality's Analog/Mixed-Signal/RF IC Design Center in Columbia, MD.

*For a copy of complete article containing all charts and images, please e-mail Web Editor at jwalkup@cahners.com.

Source URL (retrieved on 09/30/2014 - 6:25am):

<http://www.wirelessdesignmag.com/product-releases/2001/09/low-current-advantages-cmos-technologies-rfic-designs>