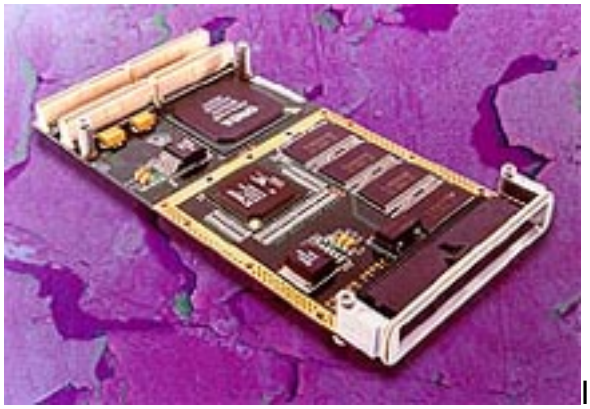
PMC Module


Ixthos announces a user-programmable and highly flexible PMC card that allows the designer to uniquely configure the module to meet virtually any I/O need for telecommunications applications and for increasing the computing performance of CHAMP-based DSP sub-systems.
The new PMC GPIO-1&#153 provides time-critical wireless and wireline telecommunications applications with additional, high performance, front-end processing &#151 without the need for a dedicated DSP &#151 to quickly and cost effectively implement those application-specific functions. The PMC GPIO-1 provides a 300K gate programmable FPGA and 64 user-defined, bi-directional, single-ended or differential I/O lines, with each signal presenting the option of driving or receiving LVDS, LVTTL, CMOS, and other levels, with on-board network termination. The GPIO-1 presents a high performance, 64 bit wide, 66 MHz PCI interface to the baseboard with up to 256 MB of on-board SDRAM memory and furnishes self-hosted DMA and interrupt capabilities.
Intelligent FPGA cores &#151 available from Xilinx&reg and other multiple third party vendors &#151 allow the implementation of enhanced DSP co-processor and hardware accelerator functions, such as convolutions and filtering, which are ideal for wireless baseband applications. Also available are intelligent FPGA cores to implement FIR and IIR filters, error correction (Reed-Solomon, Viterbi, etc.), ADPCM Modems, MPEG decoders, Ethernet MAC, HDLC controllers and more. With the proper intelligent cores, the PMC GPIO-1 can meet many International Communications Union (ITU) H.xxx audiovisual and multimedia and G.xxx transmission and networking algorithms/codes standards.
In addition, the new GPIO-1 software developer's toolkit provides users with a CD-ROM containing a comprehensive series of license-free software programming examples and built-in-test loopback test hardware for high reliability telecom applications. Also included are VxWorks board support packages and drivers, FPGA configuration files and royalty-free Verilog RTL design sample code and simulation test benches for the PCI interface IxBus and on-chip FIFOs to speed code development. In addition, a built-in-test capability allows users to easily determine with high confidence if the PMC module hardware is operating within specifications. The PMC GPIO-1 Development Kit also contains sample software for implementing a high speed, buffered message-passing data port.
The dedicated, Xilinx Virtex&#153 user-programmable FPGA readily accommodates the design of custom digital interfaces for sending and receiving data through a

front panel connector or to the backplane. An 80-pin, pre-terminated flat ribbon cable is provided for mating with the standard, 80-pin header for front panel I/O for fast system I/O prototyping and custom development.

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