

LVDS Enables High-Speed Signal Distribution in 3G Basestations

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3G mobile communications such as W-CDMA, EDGE, and CDMA2000 promise the magic of media-rich, high-speed Internet access at your cell phone. To service this bandwidth, the cellular basestations (which interface wireless handsets to the wireline networks) will process and distribute exponentially greater amounts of digital data. Inside the basestation, this data will move at high speeds across backplanes, through cables, and within circuit boards. Low Voltage Differential Signaling (LVDS) will be the signaling standard of choice for delivering this data while minimizing space, noise, and power critical constraints for basestation designs. This article discusses data and clock distribution applications using LVDS serializers, deserializers, multiport repeaters, crosspoint switches, and level translators. The focus will be on LVDS circuits, architectures, and specifications that are most relevant to 3G basestation design.

LVDS is a physical layer data interface standard defined by the TIA/EIA-644 and the IEEE 1596.3 standards. It is designed for high-speed, low-power, and low-noise point-to-point communications, typically over balanced, controlled-impedance media of 100 missing code. Like other differential signaling standards, LVDS radiates less noise than single-ended signals due to the canceling of magnetic fields, and is more immune to noise because it is coupled onto the two wires as a common-mode signal (i.e., equal levels of noise appear on both lines). In addition, LVDS drivers use a current-steering output configuration (Figure 1), which reduces ground bounce and eliminates shoot-through current compared with voltage-mode drivers used in other differential signaling standards. Reduced voltage swing (only missing code 350 mV versus missing code 800 mV for PECL and missing code 2 V for RS422) allows LVDS to achieve data rates comparable to PECL (800Mbps) while dissipating only one-tenth the power. This combination of high speed, low power, and low noise make LVDS the ideal signaling standard for distribution in 3G basestations.

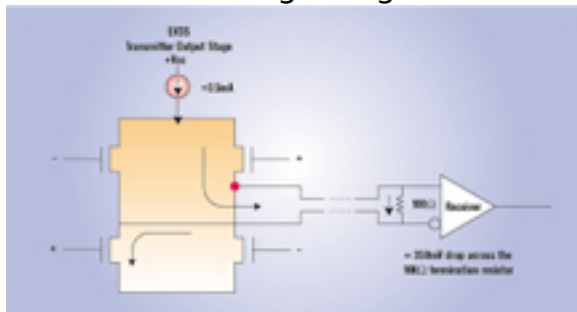


Figure 1. LVDS current-steering output stage transmits data differentially to a remote receiver.

In addition to the benefits discussed above, LVDS serializers and deserializers will also contribute enormous space and cost savings to basestation designs. To service the bandwidth required in 3G networks, new basestations will require a greater number of cards compared with 2G systems especially baseband cards, which perform the heavy digital signal processing required for spread spectrum,

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interleaving, and error control techniques. As data throughput increases between these cards, traditional TTL backplanes will no longer be sufficient because (1) TTL cannot switch at high enough speeds, and (2) wide parallel buses require large and expensive backplanes, which increase system size and cost. The MAX9205 serializer and MAX9206 (future product) deserializer from Maxim Integrated Products solve this problem by converting 11 TTL lines (10 data + 1 clock) into just one high-speed LVDS pair (Figure 2). This reduces interconnect by 5 times. In basestations with high card counts, such as 3G systems, these products translate to an enormous savings in space and cost.

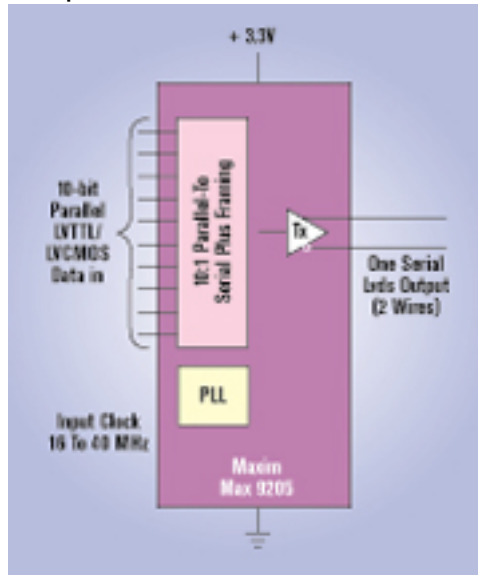


Figure 2. The MAX9205 serializer reduces the number of interconnect lines by a factor of five.

The MAX9205 serializer converts 10-bit wide parallel LVTTTL/LVCMOS data into an LVDS serial data stream. A high-state start bit and a low-state stop bit, added internally, frame the 10-bit parallel input data and ensure a transition in the serial data stream. Therefore, 12 serial bits are transmitted for each 10-bit parallel input. The MAX9205 accepts a wide 16 - 40 MHz reference clock to produce a serial data rate from 192 Mbps (12 bits \times 16 MHz) to 480 Mbps (12 bits \times 40 MHz). However, since only 10 bits are from input data, the actual throughput is 10 times the reference clock frequency. The MAX9206 deserializer receives the serial output from the MAX9205 and converts it back to 10-bit-wide parallel data. Because the deserializer recovers both clock and data from the serial data stream, clock-to-data and data-to-data skew that would be present with a parallel bus are eliminated. Together, the MAX9205 and MAX9206 form a complete solution for reducing card-to-card interconnect. The partitioning of these functions into two ICs, versus a single integrated SERDES, is ideal for 3G basestations, which commonly employ unidirectional links. For example, a "baseband receive" card might be dedicated to performing signal processing on data that is received from a radio transceiver card. In this case, only deserialization would be required on the baseband card. Therefore an integrated SERDES would consume extra space and cost versus a standalone deserializer.

In basestations already employing serialized backplanes, an LVDS multiport repeater can further reduce board space and cost. Most basestation architectures contain cards that must broadcast or transmit their data to multiple destination cards. For example, many systems employ multiple baseband cards in parallel to

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process received data from a single radio transceiver card. The brute force implementation of this architecture would require the radio card to include as many serializers as there are deserializers on the destination baseband cards (Figure 3a). By using a multiport repeater such as the MAX9150, this serializer count can be dramatically reduced by as much as 10:1 (Figure 3b). When used with a single serializer, the MAX9150 replaces 10 serializers with only one. This architecture is effective only with multiport repeaters specified with sufficiently low jitter. Jitter, the deviation from the ideal timing of an event or signal edge, prevents the deserializer from successfully recovering clock and data from a serial bit stream. The jitter budget for a typical LVDS serializer/deserializer pair can be as low as several hundred picoseconds. This budget is further reduced by jitter resulting from traces, cables, and connectors in the signal path. Therefore additional devices in the signal path between a serializer and deserializer must exhibit extremely low jitter. With only 120ps maximum peak-to-peak maximum jitter, the MAX9150 guarantees lower jitter than any multiport repeater on the market.



Figure 3a. A broadcast topology is here implemented via the brute force method of using ten LVDS serializer ICs. Figure 3b. The MAX9150 multiport repeater frees up board space by eliminating the serializer ICs.

In other parts of the high-speed serial signal path, basestation architectures often require simple switching, multiplexing, and repeating functions. As in the example of the multiport repeater, these functions must be provided with minimal impact to the jitter budget. The MAX9152 2 × 2 LVDS crosspoint switch provides several of these functions in one package. It includes two LVDS/LVPECL inputs, two LVDS outputs, and two logic inputs that determine which inputs are connected to which outputs inside the IC. It can be programmed to connect any input to either or both outputs, allowing it to be used in the following configurations: 2 × 2 crosspoint switch, 2:1 mux, 1:2 demux, 1:2 fanout buffer, or dual repeater. This flexibility makes the MAX9152 ideal for protection switching for fault tolerance, loopback switching for diagnostics, fanout buffering for data distribution, and signal regeneration for communication over extended distances. Ultra-low 120ps maximum peak-to-peak jitter ensures reliable communications in high-speed serial links.

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PART NUMBER	NO. OF Tx/Rx	VDD (V)	DATA RATE (Mbps)	Max. Pulse Skew (ps)	PLD Package
SINGLE TERMINAL					
MAX121	1/0	3.3	800	153	6-SO (S-SC70)
MAX122	2/0	3.3	500	153	9-SO (S-SC70)
MAX123/MAX124	4/0	3.3	800	153	14-SO (S-SC70)
SINGLE DUAL/QUAD					
MAX125	2/1	3.3	500	163	9-SO (S-SC70)
MAX126	4/1	3.3	200	163	9-SO (S-SC70)
MAX127	4/2	3.3	300	163	9-SO (S-SC70)
MAX128/15/MAX129/17	4/4	3.3	800	163	14-SO (S-SC70)
MAX125/MAX126/14					14-SO

In lower-speed signal paths, such as clock distribution networks and control buses, LVDS is also improving performance by replacing older signaling standards such as TTL and RS-422. In basestation radio transceiver cards, where there is tremendous sensitivity to radiated noise, LVDS is the ideal signaling standard for the distributing the reference clocks used by PLL frequency synthesizers. Although these circuits do not require the speed performance of LVDS (basestation reference clocks typically run in the tens of MHz), they benefit from LVDS's low power consumption and low radiated noise. Low-speed control buses, used for arbitration, handshaking, and other peripheral communications between cards, also benefit from noise and power reduction of LVDS. Level translators, used solely to translate signals between LVTTTL/LVCMOS and LVDS, provide a simple means of constructing LVDS clock distribution networks and control buses from existing LVTTTL/LVCMOS designs. Maxim's family of single, dual, and quad line drivers and receivers (see Table 1) are the ideal building blocks for such networks, as they include some of the smallest (SC70 and SOT23 packages) and lowest pulse skew devices available (pulse skew is the predominant measure of jitter in these devices).

By exploiting the benefits of LVDS in clock distribution, control buses, backplanes, and other areas of high-speed signal distribution, 3G basestations will deliver higher bandwidth wireless services without requiring proportionately greater cost, size, and power. The products discussed in this article offer these benefits not only in the form of the LVDS signaling standard, but also by way of the architectures and topologies that they enable. Comprehensive familiarity with LVDS technology, products, and applications are essential tools for any engineer developing next-generation cellular basestations.

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