Digital Signal Processor

Motorola introduced the 56L307 digital signal processor, the newest member of its DSP56300 family. A migration of the popular 24-bit DSP56307 to HiP4 technology, the DSP56L307 offers performance of 290 DSP MIPS. The DSP56307 is widely adopted in multi channel networking communications applications ranging from packet telephony to wireless digital cellular base stations. The advanced higher performance, pin-compatible 56L307 allows customers to add features to existing products or reduce their cost per channel. Since the DSP56L307 provides a 60 percent performance increase over the DSP56307, it also opens opportunities for new applications such as Integrated Access Devices (IAD), in which customers add voice capability to DSL digital data products like DSL modems.

The DSP56L307 operates at 160 MHz at 1.8 volts and features 64K words of on-chip memory. Its 160 MHz on-chip Enhanced Filter Co-processor (EFCOP) allows filter algorithms to be processed in parallel with core operations. The EFCOP provides an extra performance boost in applications such as echo cancellation, and optimizes voice quality without sacrificing channel-processing performance. This enables exemplary performance for this class of DSPs in wireless infrastructure applications.

The DigitalDNA&#153 technology in Motorola's communications, network, host, and digital signal processors enables its customers to build Smart Networks solutions for network connectivity. To help meet the needs of future services through software upgrades, these networks are built around programmable processors, such as the DSP56L307, rather than fixed function solutions. The 160 MHz DSP56L307 offers developers of high density, multi-channel communication and networking systems a DSP solution that is designed to provide higher system performance while consuming minimal power and minimal board space.

Designs based on the DSP56L307 can gain up to 80 percent processing capability over systems using comparable DSPs without an EFCOP, resulting in higher channel density per DSP device at a lower cost (without sacrificing board space or increasing power consumption. Four DSP56L307s, with 80 percent utilization of the EFCOP, produce 1160 MACS. Five memory switch options in this flexible device help designers scale the program and data to optimize their system performance.

In addition, the DSP56L307 is code and footprint compatible with other members of the DSP56300 family including the DSP56307 and the DSP56311. Existing designs based on these products can easily migrate to the 56L307, preserving a customer's investment in legacy code and hardware board design.

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