PLL Clock Drivers for High Speed Clocking Applications

Two low voltage PLL clock drivers designed for use in high speed memory clocking applications are available from Fairchild Semiconductor. Designated the FMS7950 and FMS7951, the PLL clock drivers operate at speeds of up to 175 MHz and are designed for high clock fanout and where matching requirements for skew and jitter are critical. Applications include registered DIMM memory modules and wherever common clock timing is critical in system clock distribution.

The FMS7950 operates off a crystal or oscillator input with clock multiplier; the FMS7951 accepts a PECL clock input and features zero delay and clock multiplication capability. Both parts provide nine configurable CMOS outputs with less than 250 pos of output-to-output skew and less than 300 ps of cycle-to-cycle jitter.

The FMS7950 and FMS7951 are each packaged in a 32-lead LQFP and rated for 0 to 70&#176C operation. V_{DD} range is 3.0 to 3.6 volts. A power down pin is provided for system testing.