Phase Noise PLL Family

Cypress Semiconductor introduces its Radio Frequency Phase Lock Loop (RF PLL) product family, featuring low phase noise floor, providing clearer voice and higher throughput for digital data transmission.

The CYW23xx product family, which supports frequency outputs ranging from 0.5 to 2.5 GHz, is targeted at communications systems such as broadband networks, RF base stations, wireless local loops, and cellular and cordless phone handsets.

The CYW23xx family consists of three single-PLL and six dual-PLL devices. The devices offer low phase noise floor while maintaining footprint and register compatibility with LMX23xx series of National's PLLatinum&#153 PLLs. Low noise means higher data integrity &#151 important for voice applications but critical for data communications, where bit-error can corrupt the data flow.

Cypress aims to port the RF chips to its 3.3 volt, double-layer-metal, 0.25-micron BiCMOS process.