Multi-Chip Packages

White Electronic Designs' 8M x 64 and 8M x 72 synchronous DRAM multi-chip packages, designed to complement the PowerPC&#153 and other high-performance memory controllers, are now available in registered versions that enhance performance of bus speeds at 66MHz and 100MHz.
The SDRAMs are each housed in a 219 plastic ball grid array package that saves 33-60% board space over a comparable discrete approach, and has a lower profile than other high-density memory approaches. It also reduces I/O connections by 31-40%, and provides lower inductance and capacitance for low noise performance. A High Tg laminate interposer provides optimum TCE match.
The SDRAMs are high-speed CMOS designed to operate in 3.3 V, low-power memory systems and are available at 125 MHz and 100 MHz. Each chip is internally configured as a quad-bank DRAM with a synchronous interface. The devices use an internal pipelined architecture to achieve high-speed operation; the column address can be changed every clock cycle. Read and write accesses are burst oriented.
The multi-chip packages are suitable for a wide range of telecom, datacom, and embedded applications as well as high-reliability COTS (Commercial-Off-The-Shelf) applications. Each is available in commercial, industrial, and military temperature ranges. The 64 MByte WEDPN8M72VR-XBX provides an upgrade from White's 32 MByte WEDPN4M72VR-XBX SDRAM, and is upgradeable to 16M x 72, 128 MByte density (advanced). The three products are pinout compatible.

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