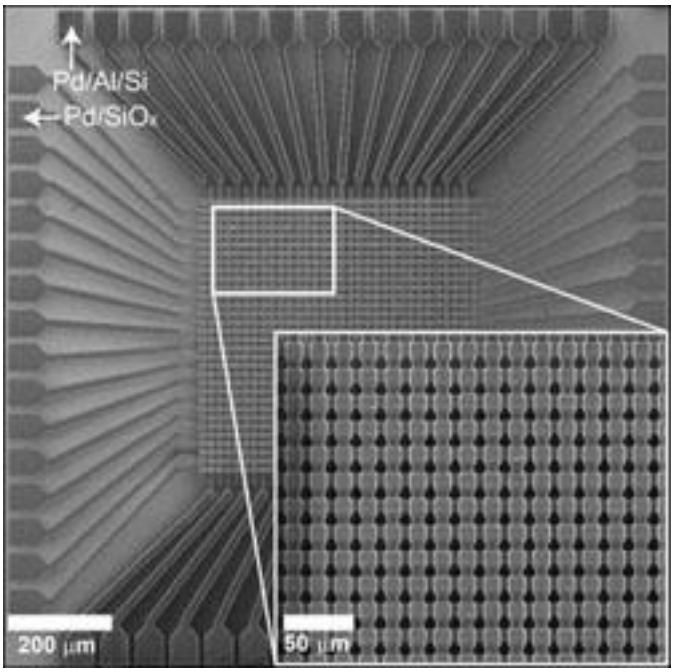
Silicon Oxide Memories Transcend a Hurdle

Jade Boyd, Rice University

Embedded diodes boost Rice University invention's potential as robust, roomy memory.



Houston – A Rice University [1] laboratory pioneering memory devices that use cheap, plentiful silicon oxide to store data has pushed them a step further with chips that show the technology's practicality.

The team led by Rice chemist James Tour has built a 1-kilobit rewritable silicon oxide device with diodes that eliminate data-corrupting crosstalk.

A paper on the new work appears this week in the journal Advanced Materials.

With gigabytes of flash memory becoming steadily cheaper, a 1k nonvolatile memory unit has little practical use. But as a proof of concept, the chip shows it should be possible to surpass the limitations of flash memory in packing density, energy consumption per bit and switching speed.

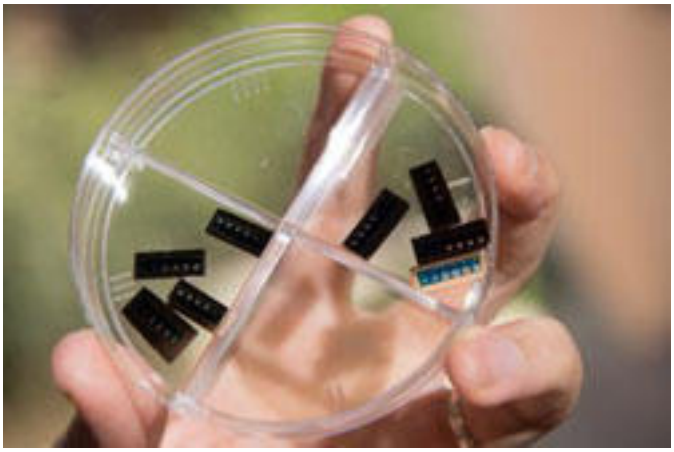
The technique is based on an earlier discovery by the Tour lab: When electricity passes through a layer of silicon oxide, it strips away oxygen molecules and creates a channel of pure metallic phase silicon that is less than five nanometers wide. Normal operating voltages can repeatedly break and "heal" the channel, which can be read as either a "1" or "0" depending upon whether it is broken or intact.

The circuits require only two terminals instead of three, as in most memory chips. The crossbar memories built by the Rice lab are flexible, resist heat and radiation and show promise for stacking in three-dimensional arrays. Rudimentary silicon

memories made in the Tour lab are now aboard the International Space Station, where they are being tested for their ability to hold a pattern when exposed to radiation.

The diodes eliminate crosstalk inherent in crossbar structures by keeping the electronic state on a cell from leaking into adjacent cells, Tour said. "It wasn't easy to develop, but it's now very easy to make," he said.

The device built by Rice postdoctoral researcher Gunuk Wang, lead author of the new paper, sandwiches the active silicon oxide between layers of palladium. The silicon-palladium sandwiches rest upon a thin layer of aluminum that combines with a base layer of p-doped silicon to act as a diode. Wang's 32 x 32-bit test arrays are a little more than a micrometer deep with crossbar line widths of 10 to 100 micrometers for testing purposes.



"We didn't try to miniaturize it," Tour said. "We've already demonstrated the native sub-5-nanometer filament, which is going to work with the smallest line size industry can make."

The devices have proven to be robust, with a high on/off ratio of about 10,000 to 1, over the equivalent of 10 years of use, low-energy consumption and even the capability for multibit switching, which would allow higher density information storage than conventional two-state memory systems.

The devices dubbed "one diode-one resistor" (1D-1R) worked especially well when compared with test versions (1R) that lacked the diode, Wang said. "Using just the silicon oxide was not enough," he said. "In a (1R) crossbar structure with just the memory material, if we made 1,024 cells, only about 63 cells would work individually.

There would be crosstalk, and that was a problem."

To prove the 1D-1R's capabilities, Wang isolated 3 x 3 grids and encoded ASCII letters spelling out "RICE OWLS" into the bits. Setting adjacent bits to the "on" state – usually a condition that leads to voltage leaks and data corruption in a 1R crossbar structure – had no effect on the information, he said.

"From the engineering side of this, integrating diodes into a 1k memory array is no

small feat," Tour said. "It will be industry's job to scale this into commercial memories, but this demonstration shows it can be done."

For more information visit www.rice.edu [1].

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