New Tech to Improve On-Chip Networks

Novel technologies are being developed to make computing processors more efficient.

Technology being developed by researchers from three universities is expected to improve next-generation integrated circuits called network-on-chip. The work will support the growing demand for computing power and could improve overall performance of multi-core processors by integrating wireless technology with copper wiring on devices.

Amlan Ganguly, an assistant professor of computer engineering at Rochester Institute of Technology, is part of the team that received an $800,000 grant from the National Science Foundation for the project. He will be working with project leader Partha Pande, associate professor of electrical engineering at Washington State University, and researchers from Georgia Institute of Technology to develop the new infrastructure that could increase the speed and reduce the power usage in today's computer processors, augmenting the on-chip network of miniature copper wires with wireless interconnects.

The on-chip wireless protocol that Ganguly will develop, called "Hierarchical On-Chip Millimeter-Wave Wireless Micro-Networks for Multi-Core Systems," will allow for multiple processing engines on the chip to communicate simultaneously using a process much like that of traditional mobile telephone networks.

This first-of-its-kind process is projected to have improved results from earlier work on a token-based protocol where access on the wireless channel is granted to only a single processor one time, he says.

"The role of on-chip networks is to communicate between multiple cores, or processors, on a chip efficiently so that they can share their results and can communicate effectively with each other," Ganguly says. "That communication has been a bottleneck over the past 10 years because the communication has been taking up a lot of energy, a lot of processing time. The major thrust in this area is to reduce that energy dissipation, to make computing systems more sustainable."

On-chip networks are subsystems on computer chips, also referred to as integrated circuits. Currently, the chips are designed with copper wiring and circuitry. The team is developing an alternative data transfer process modeled, in part, on cellular telephone technology—with single antennae capable of accommodating multiple users at one time—yet on a significantly smaller scale on the chip.

Additionally, the new protocol is expected to reduce energy consumption for computer processors that operate day-in and day-out.

"The wireless bandwidth is very limited because it is in a small, miniature scale, so it's not like a cellular network where you have thousands of cell phones working on really huge base stations," Ganguly says. "When we put the wireless nodes on a chip and they try to communicate, there has to be a way that we are sure they can communicate without interfering with each other. My goal is to design a collision-free, non-interfering wireless, medium-access protocol for the network-on-chip."

"That is a big leap in terms of usage of the available wireless resources," Ganguly says. "You lose your dependence on energy, and that pushes us toward green computing and makes it more sustainable."

Washington State University is overseeing the entire project and, in collaboration with RIT, is designing the architecture. Georgia Tech researchers are designing the on-chip antennae that will enable the wireless technology on the chip.

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