

## **Latest High-Speed Memory Controller and PHY Interface Specification Released**

The DDR PHY Interface (DFI) Technical Group today released the preliminary DFI 3.0 specification, the latest version of the pervasive industry specification that defines an interface protocol between DDR memory controllers and PHYs. The new specification enables the development of chips to support the emerging DDR4 memory standard, and is the result of collaborative work between the DFI Technical Group members including ARM Limited, Cadence Design Systems, Inc., Intel Corporation, LSI Corporation, Samsung Electronics, ST-Ericsson and Synopsys, Inc. Supported by major DDR IP suppliers, the DFI interface is in use by hundreds of companies with 3100 downloads.

"DFI has quickly become the dominant interface specification for DDR controllers and PHYs, and semiconductor companies are already specifying products to support the upcoming transition to DDR4," said John MacLaren, chairman of the DFI Technical Group. "This new specification eases the integration of DDR4 memory controllers and PHYs, taking into account the complex power and performance challenges associated with implementing high-speed memory."

Building upon the solid foundation of previous DFI specifications, DFI 3.0 defines methods for interfacing to DDR4 devices with proposed data rates up to 3.2 Gbits/second per pin -- more than 50 percent faster than the current DDR3 standard -- and extends the low-power interface that was introduced with DFI 2.1. By accounting for frequency and power challenges at high speeds, the new specification helps ensure exceptional performance in systems using DDR4 memory. The preliminary specification is available now for download at [www.ddr-phy.org](http://www.ddr-phy.org).

**About the DFI Technical Group** The DFI Technical Group is a standards organization comprised of leading semiconductor companies that implement the DFI specification. The specification defines an interface protocol between memory controller logic and PHY interfaces, with a goal of reducing integration costs while enabling performance and data throughput efficiency. The protocol defines the signals, timing, and functionality required for efficient communication across the interface. The specification is designed to be used by developers of both memory controllers and PHY designs, but does not place any restrictions on the how the memory controller interfaces to the system, or how the PHY interfaces to the DRAM devices. For more information about the DFI specification, its community, activities and how to participate, visit: [www.ddr-phy.org](http://www.ddr-phy.org).

**What Member Companies are Saying about the DFI 3.0 Specification:**

"As a founding member of the DFI Technical Group, ARM continues to support the

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Published on Wireless Design & Development (<http://www.wirelessdesignmag.com>)

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initiative to build standard specifications for DDR4 memory," commented John Heinlein, vice president marketing, Physical IP Division at ARM. "Since ARM provides DDR PHY and memory controller subsystems, we understand the importance of providing customers with a framework to improve interoperability and verification."

"As the leading supplier of DDR memory IP, we are starting to see strong demand for solutions that will ease the development of DDR4 products," said Vishal Kapoor, vice president, marketing, SoC Realization at Cadence. "We will therefore continue to drive the development of the DFI specification, and to enrich the DFI-enabled ecosystem with products like DFI 3.0 compliant DDR4 memory controllers, DDR4 PHYs and DFI verification IP. These products will be a requirement for customers designing advanced-node solutions."

"As the complexity of the DDR SDRAM interface increases, the DFI specification greatly enhances designers' experiences with subsystem integration," said Derrick Butt, principal engineer, Network and Storage Products Group at LSI Logic. "As one of the early adopters and contributors on DFI standards, LSI has greatly reduced the memory interface subsystem development effort for our customers. LSI will continue to work with industry experts on the committee to enable customer success."

"Synopsys' active participation in the DFI 3.0 committee enables us to extend our successful track record of developing comprehensive DesignWare(R) DDR controller and PHY IP solutions that reduce designers' risk and ease their integration effort," said Navraj Nandra, senior director of marketing for mixed-signal and analog IP at Synopsys. "As a leading provider of DDR interface IP, Synopsys continues to support the latest DDR technologies with high-quality IP products that enable designers to meet the stringent power, performance and latency requirements of today's advanced SoC designs."

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**Source URL (retrieved on 03/14/2014 - 4:48am):**

<http://www.wirelessdesignmag.com/news/2011/09/latest-high-speed-memory-controller-and-phy-interface-specification-released>