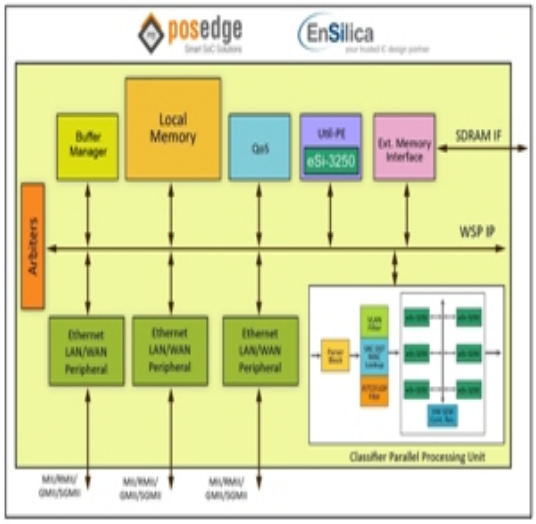
Posedge selects EnSilica’s processor for innovative 7-core Gateway SoC



EnSilica, a leading independent provider of front-end IC design services, has announced that Posedge, a semiconductor intellectual property and solutions provider based in Sunnyvale (California, USA), has licensed its high-performance eSi-3250 32-bit processor core for an innovative, new Residential and SMB Gateway solution that performs Wire-Speed Routing at multi-gigabit rates. Posedge will initially use its next generation Residential and SMB Gateway processor in a 40nm SoC project it is currently developing for a customer. Posedge is using both EnSilica's Windows and new Linux-based toolchain to underpin the development process. Posedge's new Residential and SMB Gateway processor is an innovative, 7-core design that utilises six eSi-3250 cores as identical datapath processors performing such functions as packet classification and packet editing, and another as a utility processor implementing high level functions, IPSec software and TCP offload. Posedge chose the eSi-3250, the top-end core in EnSilica's eSi-RISC family of processors, following an extensive evaluation of three different CPU cores, as it exhibited the best cost/performance metrics. "Of the three processors that we evaluated, the eSi-3250 was a clear winner, proving extremely conducive to the implementation of multicore SoCs," said Chakra Parvathaneni, Vice-President of Marketing for Posedge. "EnSilica has provided us with an extremely flexible set of cores in the configurations required to deliver the functionality we need within a single SoC. The eSi-3250 is also backed by a toolchain capable of supporting multicore debug and validation. We are now actively looking to use the eSi-RISC family in other solutions we are developing, including a new 802.11 WLAN MAC/PHY solution. Several key factors were crucial to Posedge's choice of the eSi-3250 for its Residential and SMB Gateway processor – performance, code density, silicon area, ease of integration and EnSilica's flexible licensing model. Performance is critical to Packet Processing applications and especially in this target application to achieve a line rate at 2 Gbps. With performance typically measured in terms of DMIPS, the eSi-3250 delivers 1.2 DMIPS per MHz with a core speed of 500 MHz in Posedge's target 40nm process. The eSi-3250's high code density is also well-suited to Posedge's application, with the benefits of its high code density being

multiplied by the seven cores used. The eSi-3250's high code density is achieved through the ability to intermix 16-bit and 32-bit instructions, with all of the commonly used instructions encoded in 16-bits. The eSi-3250 also significantly reduces the silicon area in Posedge's design. As the cores were configured to Posedge's precise requirements, with unwanted features optimized out of each core, significant silicon area savings were achieved in its 7-core design. EnSilica's cost-effective and flexible licensing model has also given Posedge a distinct commercial advantage in the market. It uniquely allows them to include multiple instances of the full-featured eSi-3250 in the licensable Residential and SMB Gateway IP it sells to other semiconductor companies in the PON, Cable and DSL markets, without their customers requiring a separate license for third party processor cores. The eSi-3250's AXI interface and the proven eSi-RISC toolchain have also eased integration, enabling a rapid and smooth transition to EnSilica's eSi-RISC family of cores. "Where silicon area and performance are important, our eSi-RISC family of processors has once again shown it can deliver even for the most demanding multicore and high performance networking applications like Residential and SMB Gateways," said Ian Lankshear, Managing Director of EnSilica. "The eSi-3250 was a clear winner in Posedge's evaluation, giving them a high performance solution with excellent code density, minimized silicon area, low gate count and an easily maintained C/C++ code capability for future developments and upgrades. Our flexible licensing model also puts them in a commercially advantageous position in the market. EnSilica's eSi-RISC family provides a range of high quality, highly configurable embedded processors that are easy to integrate. The processor subsystem is delivered fully targeted to customers' ASIC technology, thereby reducing the integration effort. eSi-RISC processors provide the flexibility to define a range of hardware functions to optimize the silicon area. On–chip memory requirements are reduced through inter-mixed 16-bit and 32-bit instructions, resulting in good code density without compromising performance. It is the only processor scalable from 16-bits to 32-bits, starting from as low as 8.5k gates. eSi-RISC utilizes the industry standard GNU optimizing C/C++ compiler and Eclipse IDE for rapid software development, and supports efficient debugging on the target through a JTAG interface and hardware breakpoints. The development suite is common to both 16-bit and 32-bit processors, protecting users' software investment. For further information about EnSilica, visit http://www.ensilica.com. eSi-RISC product information and downloads can be found at http://www.esi-risc.com.