Partnership Enables Complete, Seamless Flow to Reduce Dynamic and Leakage Power in SoCs for 40nm and Below

Calypto® Design Systems Inc. announced its collaboration with Virage Logic Corporation, and the Semiconductor Technology Academic Research Center (STARC) to dramatically reduce on-chip SoC power.

Extending its ongoing, independent efforts with STARC and Virage Logic, the multi-technology collaboration resulted in the development of a seamless flow for designs with various functional modes that control multiple on-chip power domains to achieve dramatic power savings. Initial results show up to 50 percent dynamic power reduction and up to 40 percent leakage power reduction in embedded SoC memories using Calypto's PowerPro MG tool and Virage Logic's SiWare™ Memory compilers.

"Design teams are confronted with constant pressure to reduce SoC power. Without an automated flow to reduce memory power, designers are forced to engage in time-consuming analysis and error-prone manual modifications to the design," said Nobuyuki Nishiguchi, Vice President, General Manager, Development Department-1 at STARC. "Incorporating Calypto's PowerPro MG and Virage Logic's SiWare Memory IP into our low-power flow will enable designers to meet their design power goals in order to focus resources on bringing new levels of innovation to their products."

Using Calypto's patented sequential analysis technology, PowerPro MG (for Memory Gating) constructs new memory gating logic that works in conjunction with the low-power memory modes in Virage Logic's SiWare Memory compilers to produce the lowest power memory implementation possible.

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