# The U.S. Market & Design for Test

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Because many high-volume printed circuit assemblies are sent outside the United States, it is challenging to test the lower volume/high turnover assemblies domestically. But this does not need to be a problem — some simple planning and the right contract manufacturer (CM) can solve this issue.

The challenge is that the US market is made up of high-technology/low production quantity assemblies. In many circuit beds of nails cases, test is not an option because of development time, cost and the difficulty associated with finding a place for a 30-40 mil test point. These same test points also create significant EMI concerns for most electrical engineers. The challenge is to find a way to thoroughly test a fully populated circuit in a timely, cost-effective way without compromising signal integrity.

Depending on the technology, the challenge can be as simple as making minor design changes that can happen at the gerber level to requiring a significant revision to the board in question. First let’s conquer the simple. For analog, RF and lower technology digital boards the approach is the simplest. Typically, straightforward flying probe test is the answer. The better EMS companies use a dual -sided flying probe tester. For this test approach, the test engineer simply asks that the vias not be covered with soldermask, which can be a simple change handled at the CAM/gerber level.

Depending on the test coverage, the test department may recommend adding vias, assuming your design can handle it from an electrical perspective. If, as in sensitive analogs or RF technology boards, vias are being avoided the tester may be able to test at the solder joint. Allowing this requires customers to be open minded about

“witness marks” left behind by the tester. Harder solder – for example lead-free –reduces this problem. Testing this technology typically results in some of the higher test coverage approaching 100 percent.

High-technology product can create more of a challenge. The technology in this class includes high-speed digital, via in pad, blind buried vias and high BGA count. The unknown in this case is the number of circuits that actually never see an external via, making it impossible to probe the circuit. The previous guidance still applies: Have a via exposed for every circuit.

This includes making sure they are not covered by a component or soldermask. Typically, this results in adequate test coverage, but no one wants to be just okay.

Superior test coverage on this type of product includes the use of boundary scan (JTAG) technology to significantly increase the test coverage as well as reduce test time. This assumes that the components on the board are boundary scan capable. Presuming this is the case, the five signal boundary scan daisy chain circuit must be connected. Since this is for test purposes, the electrical engineer does not connect them. Instead it is done as a method for programming components. It is important to note that the original intent of boundary scan was to test and not program; however, it is used more often for programming.

Implementing boundary scan for test can be no different than your current programming routine. Simply connecting the chain opens up the possibility of test, which is a great beginning. However, it is recommended that a test engineer who specializes in boundary scan test review your schematic before you begin layout. Doing so typically will yield a faster, more thorough test. Test throughput also increases by removing all circuits tested at boundary scan from the flying probe test program. This approach has been used on boards with more than 35,000 test points, which resulted in 95+ percent test coverage.

So the challenge has been met. It is possible to have a highly tested product built in the United States at an affordable price. What has been described here requires less upfront and design work than the traditional bed of nails in-circuit test and can be used in all phases of development, including prototype, pilot and production runs.

W. Scott Fillebrown, President & CEO of ACD, became a stockholder in January 1995. Starting with ACD after college, he has a total tenure of more than 20 years with the company. He graduated from the University of Texas - Dallas in 1989 with a B.S. in Business Administration with a concentration in Marketing. Currently, he is responsible for the company’s finance, manufacturing operations and marketing efforts. Scott’s out of the box thinking towards manufacturing has led ACD to win numerous awards for revenue growth and technology advances.

Founded in 1984, ACD is a full service EMS company. The company’s services comprise complete board layout, DFM/DFA capability, printed circuit fabrication, component procurement, thru-hole, SMT and part-on-part mixed technology assembly, box build, rework, flying probe, functional and JTAG test, and

development. For more information, visit www.ACDUSA.com [1].

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