Chip Package System Convergence Requires Holistic Approach to Design and Verification

New technology trends and complex design requirements necessitate revisiting the way the industry approaches IC design and validation. With extreme demands on power, performance and regulatory specifications, it becomes essential to view the chip, package and system as a cohesive network of interdependent parts. Old “silo” based approaches founded on over-designing for margins, where chip, package and system designs proceed as independent projects, is no longer the best way to meet the performance and power requirements of today’s designs and conform to thermal and EMI specifications.

In an old silo environment, each design team works on their specific component allowing sufficient margin for cross-domain impact. For example, when signing off a chip for voltage drop, the traditional method uses a “DC or static analysis” flow with a 10 percent margin, which is two to three percent for regulator tolerance, two to three for PCB/package drop, and approximately five percent allocated for chip-level drop. Similarly, package design teams have used a heuristic-based model of the chip when designing the package.

However, this type of approach can only lead to unnecessary over-design and additional costs. It can also expose the integrated system to failure caused by cross-domain issues. For example, the impact of the package inductance on the on-chip voltage noise level can be quite severe. Unless chip designers include an accurate model of the package in their chip-level “dynamic” simulations, they will not be able to account for this effect. Similarly, package designers must have an accurate electrical model of the chip that captures varying switching currents along with parasitics on the chip, when validating the power delivery network (PDN) structure of the package. A “decoupled” approach also impacts the prediction of jitter levels at the I/O signal interface.

Traditionally, board designers use IBIS models for the I/O circuits, along with package and PCB trace information to predict timing and jitter. However, by using

this approach several critical factors can be missed that affect the signal transmission, including the variation of the supply voltage from one cycle to another, the simultaneous switching noise (SSN) coming from the transition of a large number of I/O buffers, the noise coupling between power/ground and signal traces in the package and the PCB, and layout issues in the I/O ring power/ground network.

The final success of an electronic system is contingent on its functionality at the specified operating frequency and meeting its thermal, EMI and other design requirements. An electronic system, such as those targeted for mobile handsets or servers, consists of several components including ICs, discrete components such as capacitors and inductors, power supply modules, regulators, cooling/heat sinks, etc. Even though there may be several packaged discrete ICs assembled on a printed circuit board (PCB), the key ones are typically those executing most of the application and data processing functions, such as processors and memory chips. These ICs consume most of the power in the system, transfer most data to and from their I/O circuits and have the most detrimental power, thermal and EMI signatures

In this proposed methodology to help enable chip-package-system design convergence, models are created by each design team for every step of the design process. Since it is difficult to encapsulate in one single model the various pieces of information needed for all the system-level analyses, different models must be created for application-specific analyses such as power, signal, thermal and EMI. These models capture the information that is available for each phase and specific component of the design. A comprehensive chip-package-system validation flow requires an accurate model for each component to enable cross-domain data sharing before the chip, package or system is manufactured; avoiding guess-work and the use of heuristics to predict the performance of the combined system.

By using advanced modeling and proven simulator technologies, from companies such as Apache and ANSYS, a new approach for chip-package-system convergence changes outdated compartmentalized chip, package and system design methodologies. This enables an intelligent, integrated, chip-aware system design that addresses power and signal integrity, EMI/EMC, and thermal and stress challenges.

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