Enabling Low Cost, Low Power Wireless Heterogeneous Networks

Deepak Boppana, Senior Strategic Marketing Manager, Lattice Semiconductor

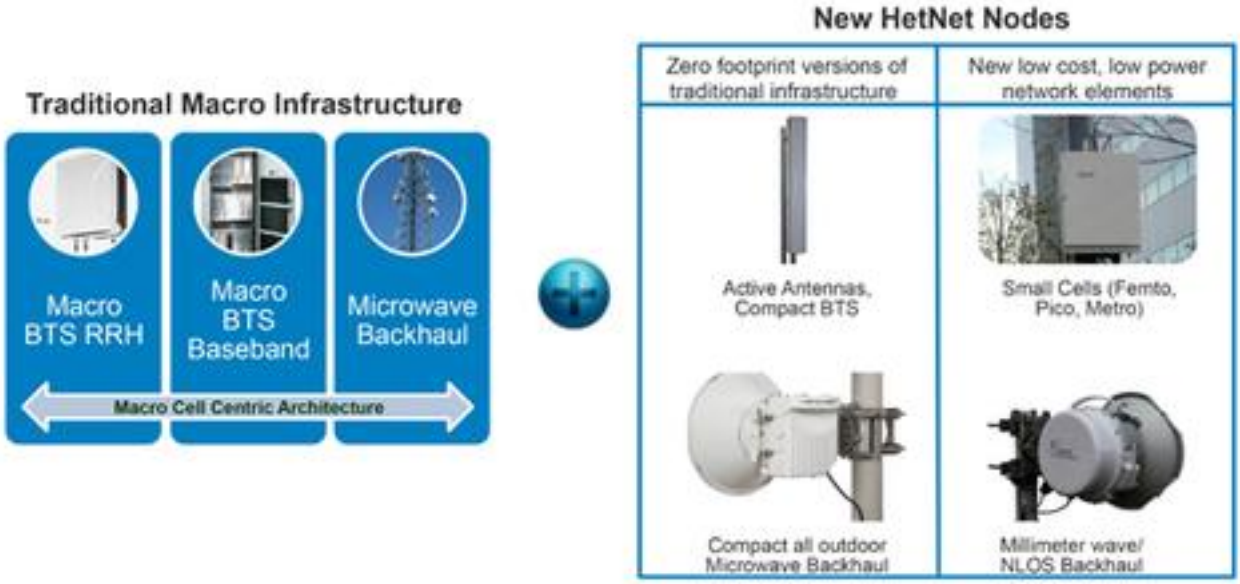
Careful partitioning of HetNet small cell architectures helps designers meet cost, power goals.

San Jose, CA – Driven by the need to address the explosive growth in mobile data and video traffic, the wireless infrastructure market is rapidly evolving toward a new Heterogeneous Network (HetNet) architecture in which the traditional macro infrastructure is supplemented by a new class of low power nodes (LPNs) such as small cells, low power remote radio heads, and relays.

At the same time, escalating demand to lower CAPEX and OPEX costs for mobile operators is driving the traditional macro infrastructure elements towards “zero footprint” architectures such as compact base stations, active antennas, and all-outdoor microwave/millimeter wave radios.

In the world of HetNet, operators have highly flexible network deployment options to make full use of their limited spectrum assets, while consumers have ubiquitous broadband coverage in a wide variety of environments.

But the question remains, can developers build and deploy scalable green HetNets capable of addressing increasing traffic requirements, including the anticipated demand from the internet-of-things (IoT), and still meet stringent cost and power targets to ensure a reasonable ROI for operators.



Common Requirements

From a hardware perspective, most of these new network elements must meet a

number of common requirements. The compact, low weight, high-volume nature of the LPNs demands stringent power consumption, board space and cost limitations. Additionally, these LPNs must be highly configurable to support multiple air interface standards and RF frequencies.

They must also be flexible enough to support in-field upgrades as new LTE-Advanced HetNet features are finalized in 3GPP Rel 11 and beyond. Ease-of-maintenance and reliability are other key requirements, including the need to support self-organizing networks (SON) capability, offer uninterrupted service during brownouts, and provide multiple network timing and synchronization options such as IEEE 1588v2 and SyncE.

Recently, semiconductor vendors have begun to address these system challenges by delivering a number of innovative baseband and RF products to address the needs of the HetNet market. Typically hardware designers use off-the-shelf ASSP solutions and/or custom ASICs to implement the data-path intensive functions because they provide the best combination of cost and power consumption required in these systems.

Similarly, design teams opt for highly integrated multi-band RFICs and wideband PAs (Power Amplifiers) to reduce RF component count on the board and help minimize overall size and weight. In addition, engineers employ a number of integrated programmable power management devices to simplify board management design by integrating programmable analog and logic to support common functions including power management, digital housekeeping and glue logic.

The following section of this paper describes the typical hardware architecture of a HetNet small cell and explains how, using some of the latest products from semiconductor vendors, designers can partition the data path, control path and power management functions to optimize performance and meet demanding HetNet requirements.

Small Cell Architecture Partitioning

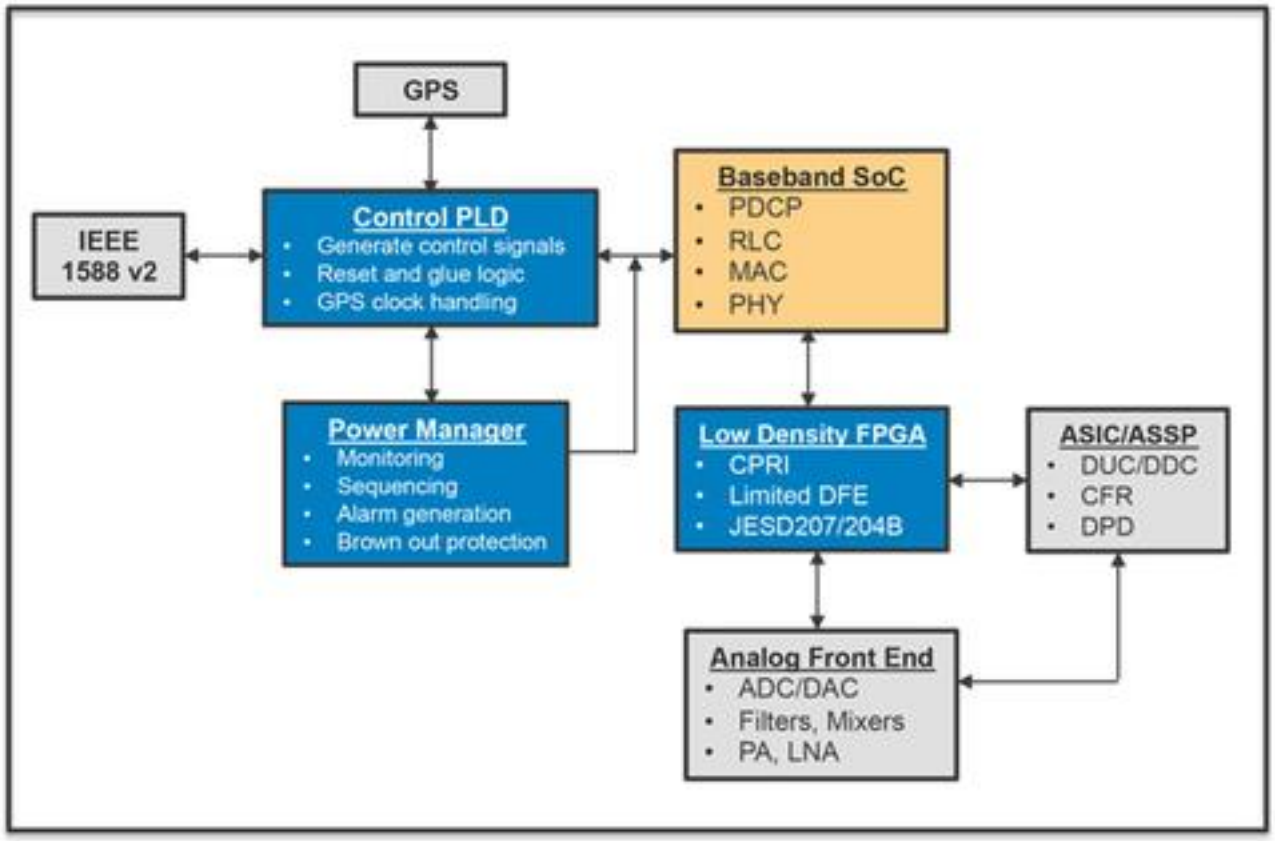
There are various types of small cells in a heterogeneous network, ranging from traditional Femto cells deployed in residential and enterprise units, to a new class of Pico and Metro cells for higher capacity and coverage (both indoor and outdoor). These small cells differ from larger macro cells in both their coverage area and average output, transmit power. For example, a small cell’s typical output, transmit power ranges from just a few hundred mW to less than 10 W.

Given the small cell’s need to support plug-and-play installation in public areas such as lamp posts, features such as size, weight, power consumption, heat dissipation and SON capability become key design considerations.

These small cells must also support different deployment configurations including compact base stations with integrated baseband and radio units in the same physical enclosure, as well as Cloud RAN type configurations where multiple

discrete radio units are connected to a common centralized baseband unit that implements LTE-Advanced capabilities such as Coordinated Multi Point or CoMP.

Figure 2 provides an overview of the high level functional blocks typically implemented in a Pico or Metro cell.



- As illustrated in figure 2 above, baseband processing including L1/L2/L3 layers is usually best suited for implementation on a baseband system-on-chip (SoC) ASSP. The SoC typically features multiple DSP and RISC cores to process software oriented functions, as well as hardware accelerators to address computationally intensive tasks found in standards such as 3G and LTE.
- In low power femto cells (~100-200mW), the data from the baseband SoC is usually routed directly to the RF analog front end via the JESD207 interface.
- Indoor Pico cells (~1W), on the other hand, usually require some limited digital front end (DFE) functionality such as crest factor reduction (CFR). These solutions also demand additional connectivity to interface to the baseband SoC via CPRI and to the data converters via LVDS/JESD204B. Low density FPGAs that combine high speed logic with SERDES and flexible IO interfaces, as well as DSP capability in a small footprint package, such as Lattice Semiconductors' ECP3-70 (ECP3 family of) devices, offer an ideal match for this application.
- Metro cells (~5-10W) typically require a full DFE solution including power amplifier (PA) linearization techniques such as digital predistortion (DPD), in addition to enhanced DUC/DDC/CFR functionality. From a cost and power consumption stand point, it makes sense to harden the computationally

intensive data path functions (DUC/DDC/CFR/DPD) in an ASIC/ASSP, while retaining the programmable connectivity functions (CPRI, JESD204B, LVDS etc.) in a low density FPGA such as Lattice's ECP3-35.

- The analog front end in femto cells and indoor pico cells is usually a highly integrated multi-mode, multi-band, multi-antenna RF transceiver chipset that includes the data converters, frequency synthesizers and channel selection filters. The analog front end for metro cells presents a more complex challenge. Designers typically combine multiple discrete higher performance components such as JESD204B based data converters and additional analog circuitry to implement PA efficiency improvement techniques such as envelope tracking.
- Time and frequency synchronization are critical for small cells and, given potential reception issues with GPS at indoor locations, backup synchronization solutions such as IEEE1588v2 or SyncE are usually implemented using off-the-shelf ASSP chipsets. To manage and distribute the clocks to the other components on the board as well perform basic control functions, IO expansion and glue logic functionality, designers typically use a small, low cost PLD such as the Lattice XO2.
- Metrocells need to support a wide range of power supply options and withstand frequent brown-outs without dropping calls. To implement multiple board level functions including power supply sequencing, monitoring, voltage measurement and power-ride-through control for brown out protection, designers need an integrated power management device such as the Lattice Power Manager II. Programmable, high precision, mixed-signal solutions such as these provide a complete power management solution, and, by replacing multiple ICs, can also improve reliability and accelerate time-to-market.

Conclusion

Clearly the future of the wireless infrastructure lies in heterogeneous networks. These innovative architectures promise to lower CAPEX and OPEX costs for operators, while delivering ubiquitous mobile broadband connectivity to consumers and to the internet-of-things.

To achieve that goal, however, designers will have to find a way to efficiently balance the system level architectural tradeoffs involved in the development of new low cost, low power network elements such as small cells, active antennas and millimeter wave radios. By utilizing the latest advances in off-the-shelf ASSPs, custom ASICs, low density FPGAs and integrated power management devices, designers can now build platforms that offer a new level of performance, integration and design flexibility without violating their stringent cost and power consumption budgets.

About the Author

Deepak Boppana is a senior strategic marketing manager at Lattice Semiconductor and has over 10 years of strategic marketing and business development experience in the mobile wireless infrastructure segment.

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