Addressing Bandwidth Challenges with LTE and MIMO

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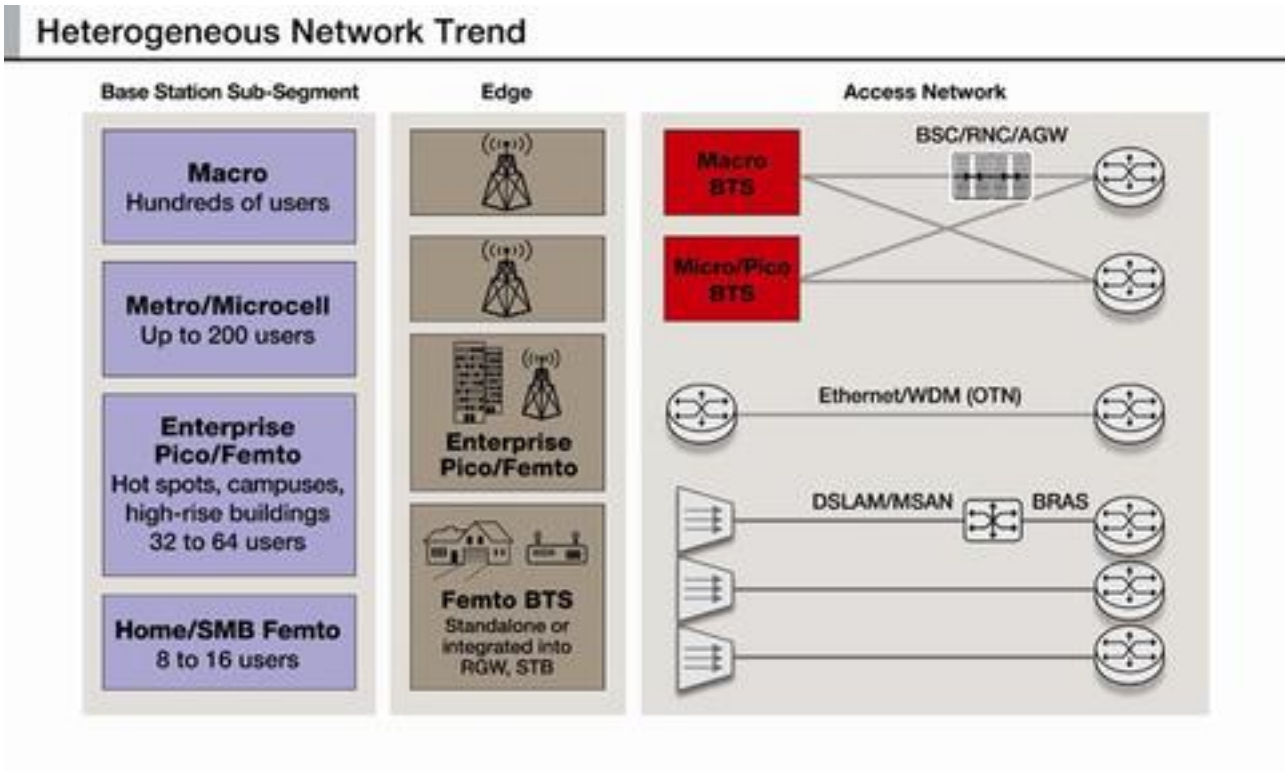
Next generation base station processors help address bandwidth challenges.

The sheer number of smart connected devices with data-intensive applications, such as high-definition video, has created an explosion in the demand for mobile broadband. This trend increasingly requires wireless infrastructure equipment manufacturers and wireless service providers to dramatically boost network performance while controlling capital expenditure, increasing power efficiency and supporting the emergence of both new technologies and form factors.



From the service providers' perspective, the key driving wireless network topologies is their ability to meet demand for high bandwidth, support dense user clusters, provide guaranteed quality of service (QoS) and minimize the associated network costs. Reaching 6.3 exabytes per month by 2015 (a compound annual growth rate of 92 percent from 2010 to 2015) 1, the current explosion in mobile data traffic worldwide provides unique challenges and opportunities for wireless infrastructure equipment manufacturers as they race to meet service providers' needs to increase capacity and create revenue growth capabilities.

Long Term Evolution (LTE) and LTE-Advanced (LTE-A) are widely accepted as the wireless technologies needed for at least the next several years to address the ever-

growing requirement for mobile data bandwidth. According to research firm Gartner, mobile connections served by 4G LTE technology worldwide will grow at a CAGR of 133 percent over the next five years and will represent six percent of all connections worldwide by 20162.

There are a number of challenges tied to deploying and managing LTE, including availability and efficient use of spectrum, interference and hand-off issues between cells and networks (leading to QoS issues), as well as future-proofing of infrastructure investment. Achieving the required capacities, QoS and lower costs are contingent upon multiple factors, such as the proximity of the users relative to the base station or the transceivers, the number of users in a cell, data throughputs and use patterns, core network capabilities, capital (CAPEX) and operating expenditure (OPEX).

Due to limited coverage in dense urban areas and inside buildings, wireless networks built based on traditional macro cell sites – commonly spaced at 10 km or more, handling hundreds of users with high-power amplifiers – will no longer be sufficient to meet subscribers' demands for faster data speeds. Instead, new types of overlay network deployments are necessary to support 4G data services. This has led to a rise in popularity of heterogeneous networks (HetNet) which comprise varying sizes of cells.

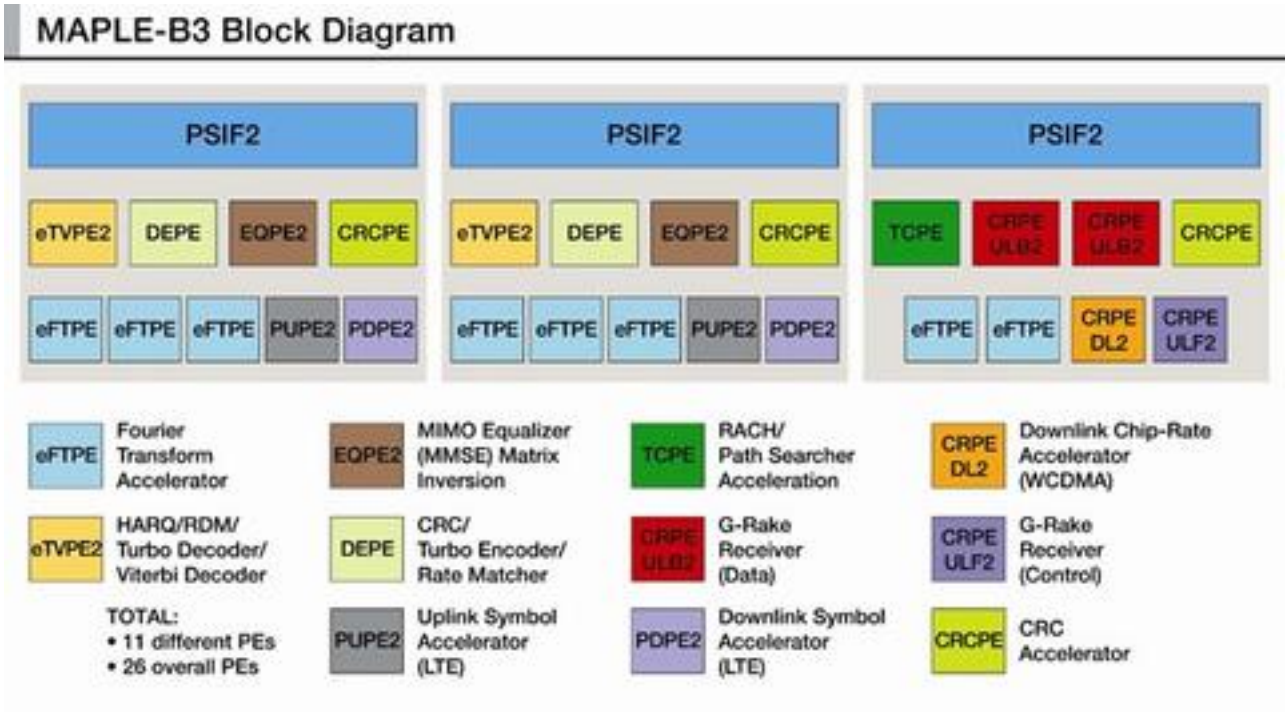
Generally, HetNets may comprise different cells: macro (wide area coverage for 1000+ users), metro (small area outdoor coverage for 100 - 200 users), pico (enterprise class for 32 - 100 users) and/or femto (SMB and residential deployment for 4 - 16 users). Often, these systems will be used in conjunction with remote radio heads (RRH) or distributed antenna systems (DAS) in order to maximize the coverage from a single small cell deployment. HetNet deployments are commonly required to be multimode capable, meaning that they can support 3G and 4G simultaneously, and should also have the capability to be upgraded to support next generation standards such as LTE-A.

Base Station Requirements

Key to any base station design are the digital baseband processing elements which define its users' capacity, data throughputs, scalability and impact on equipment and operational costs. A high degree of integration and sophistication is needed, especially for compact base station design, as is lowering the cost and power consumption of the digital processing elements while maintaining the high throughputs and capacities.

Next generation base station processors, many of which are classified as "systems on a chip" (SoCs), are helping to address many of the aforementioned challenges related to LTE and later LTE-A networks. These processors integrate multiple high-performance general purpose cores, with digital signal processing (DSP) technologies, as well as advanced hardware acceleration engines. This new category of "base station-on-chip" SoCs should provide low latency and high throughput communications at an affordable price and should offer multiple air interface support within a single, scalable architecture platform. The right balance

of high performance processing coupled with smart protocol offload provides the flexibility to run multiple standards while minimizing the cost and power.

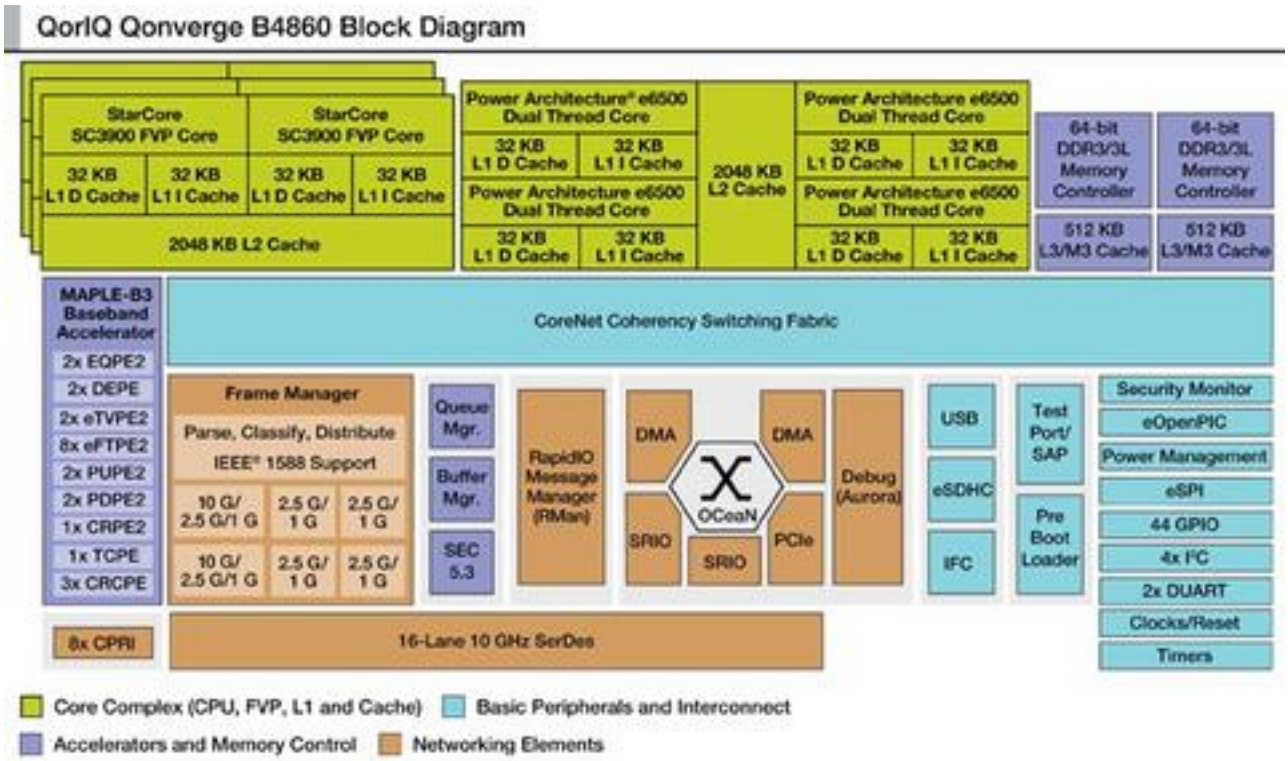


Many base station SoCs support sophisticated multiple input, multiple output (MIMO) techniques requiring a higher number of antennas. SoCs with accelerator engines are able to effectively support MIMO smart antenna technology with lower processing overhead, power and cost, providing maximum bandwidth over the available spectrum. Both HetNets and the advanced MIMO techniques supported in the LTE and LTE-A standards are key to optimizing spectral efficiency and maximizing throughput to support a growing and seemingly insatiable appetite for mobile broadband, providing as they do the maximum data rates over the air with the available frequency spectrum.

MIMO Equalization: Increasing Data Rates and Range with Base Station-on-Chip Devices

The LTE equalizer is one of the key functions in a LTE receiver and is based on a complex algebra-like matrix of multiplication, decomposition and inversion. The most advanced base station-on-chip devices are able to offload compute-intensive functions, such as equalization tasks in order to optimize performance and efficiency of the base stations supporting the LTE/LTE-A formats.

Freescale’s QorIQ Qonverge base station-on-chip devices demonstrate how offloading MIMO equalization tasks can boost performance to support LTE and other future schemes. These SoCs integrate a Multi-Accelerator Platform Engine for Baseband (MAPLE-B3) block, which includes a programmable system interface (PSIF) as well as a high-speed equalizer processing element (EQPE). The EQPE is a hardware accelerator that handles complex antenna MIMO configurations of two, four or eight in-parallel. In addition, it provides full support for a multi-core chip, in which multiple on-chip DSP cores need to be able to use a specific hardware accelerated function.



Below, the EQPE capabilities are presented in terms of low latency, high throughput and optimized control. Combined, these technologies help in LTE management and operating costs by efficiently meeting increasing data throughput requirements and delivering significant reduction in cost per megabit for the growing data traffic in cellular LTE networks.

The MAPLE PSIF completely offloads the required control and configuration of the EQPE (and all other processing elements) from the SoC's DSP cores in the physical layer implementation.

The EQPE supports minimum mean square error (MMSE) MIMO equalization as well as matrix inversion. These operations are implemented using internal floating point engines.

The EQPE features include:

1. High-precision floating point calculations: input/output samples are in block-floating; internal calculations performed using custom floating point.
2. Support for diagonal and full (Hermitian) noise and interference covariance matrix with configurable granularity.
3. On-the-fly channel estimate matrix interpolation using configurable weights.
4. Support for advanced iterative receivers (turbo-SIC):
    - Layer cancellation.
    - Rank reduction.
    - Signal covariance matrix.
5. Optimized processing order that allows for pipelining with iDFT (inverse discrete Fourier transform) operation.

6. High throughputs to provide low latency:
    - MMSE equalization: up to 425[MRE/sec] for 4x2/2x2, up to 210M[MRE/sec] for 8x2 and up to 100M[MRE/sec] for 8x4/4x4 equalization.
    - Matrix inversion:

	Hermitian	Full Matrix
2x2	240	200
4x4	96	80

Depending on the use case and assumption, the EQPE may replace up to two DSP cores at 1.2 GHz for a 4x4 MIMO MMSE equalizer, freeing the DSP cores to perform other functions. Using the EQPE accelerator, which has floating point arithmetic for increased precision, gives latency which is about three times better than the implementing the equalizer on DSP cores when normalizing for frequencies. The flagship QorIQ Qonverge SoC, the B4860, integrates six SC3900 cores running at up to 1.2 GHz, which is an equivalent of 7.2 GHz. Assuming a scenario using two SC3900 DSP cores at 1.2 GHz dedicated to a MIMO equalizer algorithm, the total capacity would be reduced by 33 percent, leaving only 4.8GHz for the rest of the Layer 1 processing. Furthermore, using the EQPE provides a lower cost and power implementation than two DSP cores.

Summary

LTE- and LTE-A-based single carrier FDMA (SC-FDMA) technology standards target much higher data throughput than current 3G technology. These higher data throughputs drive requirements for higher performance equalization blocks. To enable low latency and high throughput equalization processing required for reliable LTE communications, equalization capacity is needed to increase by factors of up to 10x compared to current 3G base station designs.

Selecting the appropriate SoC can greatly impact the ability of wireless service providers to cost-effectively manage LTE networks by meeting increasing data rates requirements and delivering quality servicer for users of cellular LTE networks. Wireless infrastructure equipment manufacturers and service providers are working closely with semiconductor vendors that provide highly integrated SoCs encompassing very high-performance CPU and DSP cores coupled with smart acceleration to offload repetitive tasks for the most efficient, lowest-power processing that can handle the growing amount of software needed to manage LTE cellular networks. By choosing SoCs from a software-compatible processor line that scales from small-cell to large-cell base station implementations, wireless infrastructure OEMs can speed development time, ease system complexity and reduce system costs.

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