Packaging and Miniaturization

Q: How can semiconductor packaging help support these new advanced technologies so that gains at the wafer level are not lost at the system level?

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The advancement of semiconductor process nodes and the demand for miniaturization creates multiple challenges for the packaging industry. In my opinion, packaging technology has consistently advanced in response to these driving forces. Lately our industry has responded to infrastructure build-outs in Brazil, Russia, India, China and emerging nations, especially mobile Internet deployments where smartphones have pushed the packaging industry to achieve aggressive size, cost, and power targets. Looking ahead to 2015, I believe that some of the most pressing industry challenges fall into five groups.

Price-Performance

Achieving price-performance goals for advanced microelectronic components requires involvement of packaging and test engineers before product development starts. Pushing packaging and test considerations into the new product introduction cycle inevitably leads to cost overruns and untimely discoveries. As product development budgets tighten in our post-recession economy, I assert that packaging and test issues must be considered in detail during product roadmapping and budgeting cycles.

To maintain alignment of packaging technologies with semiconductor advances and customer needs simply requires communication. Through roadmapping activities, corporate partnerships and industry consortia, we will continue to identify and resolve pre-competitive issues, develop standards, and evaluate the impact of technology and supply chain advances on packaging capabilities.

Design for Test (DFT)

Several decades ago, design for manufacturing became a focal point. Unfortunately, design for test is often ignored. Accessing electrical interfaces in highly integrated SiP (system in package) solutions with stacked or embedded actives is a tough proposition. Modern SiP solutions demand BIST (built-in-self-test) structures with standard interfaces to cost-effectively provide test coverage and support functional validation. Ignoring DFT is a losing proposition as a bad wafer lot, reliability and/or debug issues may quickly provide a compelling need to improve testability.

Material Stability and Precision

Modifying the thermo-mechanical behavior of packaging materials enables improved manufacturing tolerances. This allows package designers to support aggressive bandwidth specifications and increase interconnect density at lower price points. With improved manufacturing tolerances, we can predict and mitigate impedance mismatch, crosstalk, and signal switching noise issues.

Dielectric stability over moisture, temperature, and frequency is equally important for high-performance/harsh-environment applications. Coreless organic substrates using high-dielectric constant, low-loss epoxies or liquid crystal polymer are expected to enable some performance and reliability breakthroughs once substrate manufacturers can support high-precision design rules in these materials (e.g. routing a 100-ohm differential pair between 200 µm pitch capture pads with ±10% impedance tolerance, and ±5% embedded passives).

Virtual Prototyping

Design and simulation tools have come a long way. However, package designers continue to wait for commercially-available, virtual prototyping tools (i.e., an electrical design environment with integrated multi-physics simulation tools), tools for 3D package designs, and validated tools (i.e., backed by actual measurements). This limits the ability to make trade-offs and optimize packaging solutions required for first time design success.

To meet semiconductor- and customer-driven challenges through 2015, our industry must:

* Pre-qualify and ramp-up production of advanced packaging solutions, including (but not limited to) coreless organic substrates, copper wire bonding, embedded passives with tolerances of ± 5% or better, test solutions for embedded devices and signal paths, and cost-effective thermal management solutions for stacked die;

* Develop lower loss dielectrics that support tight design rules and tolerances;

* Develop integrated virtual prototyping tools that enable multi-variable trade-off analyses across different package architectures;

* Integrate back-end wafer processes into front-end packaging operations (including wafer mounting, thinning, bumping, surface activation, low-temperature bonding, wafer-level underfill/encapsulation, and damascene- compatible dicing);

* Cost-effectively develop sourcing and screening methodologies that detect and eliminate the threat of counterfeit devices in the supply chain.

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