# Serial RapidIO Gen 2 in Next-Generation Wireless Base Stations

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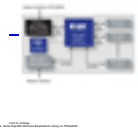
Third- and fourth-generation wireless base stations that use today's most-common interface standards, such as WCDMA, TD-SCDMA, LTE, TD-LTE and Wimax, require a large amount of signal processing to keep up with the uplink and downlink bandwidth requirements. Those standards require the use of advanced antenna systems (AAS) and multiple input, multiple output (MIMO) antennas arrangements. More antenna data is therefore transmitted to and received from the radio heads. This article describes the use of Serial RapidIO® (S-RIO®) in the base station and explores a few possible architectures. Different architectures require different S-RIO data flows and the opportunity of modeling the S-RIO traffic is discussed.

#### Architecture with One or More FPGAs

The first architecture, shown in Figure 1, uses one or more field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs) to receive and transmit antenna data typically through common public radio interface (CPRI) or the Open Base Station Architecture Initiative (OBSAI), a common antenna interface standard. This is used when the physical layer protocol (PHY) layer of the wireless protocol is implemented in the FPGA/ASIC.



[1]

Then, the data is passed through S-RIO to a bank of digital signal processors (DSPs) for the lower media access controller (MAC) layer processing of the wireless protocol. The upper MAC layer processing is done in the control processor (CP). The CP is used for quality of services (QOS) and multiple other management functions within the baseband card. It is also typically responsible for access to the network over Gigabit Ethernet links and for implementing security for public network access. Some architectures also centralize the network interface where the CP on each

baseband card would communicate with the network interface card where the security function to access the public network would be performed.

When using an FPGA in this architecture, the base station is completely software programmable and scalable. It can be described as a “software configurable base station.” System designers could increase or decrease the size of the FPGA and add or remove DSPs to get a smaller or bigger base station that could service more or less subscribers. Also, for the MIMO algorithm, designers could also group users in smaller or bigger groups, which would require more or less processing power from the FPGA and DSPs.

**Architecture Without FPGA or ASIC**

[2]

The second architecture, shown in Figure 2, does not use an FPGA or ASIC in the antenna data path, but instead, sends all of the antenna traffic to all the DSPs in the system. This is a distributed architecture. Each DSP receives the antenna data and only consumes what it requires to service the users for which it is responsible. Once the sample-level processing is done in the DSPs, the data packets can be sent through S-RIO to the control processor to and from the network.

Similarly, a lot of control traffic exists between the control processor and the DSP for QOS and management functions for each user. Serial RapidIO is ideal in architectures that utilize logical layer functions, such as direct memory transactions and/or RapidIO Messaging, which is an effective way to send a large message for up to 4Kbs. The RapidIO Messaging is a push architecture and enjoys the lowest system latency over other protocols. The Serial RapidIO switch latency is also minimal at around 100ns, creating a seamless DSP-to-DSP transfer. This architecture is also scalable and can also be described as a software configurable base station.

In the architecture illustrated in Figure 2, not only can designers easily define smaller or bigger base stations that can service more or less users, but they can also target different wireless standards with the same architecture. Only the software needs to change to make the architecture a common platform between standards.

For the architectures in Figure 1 and Figure 2, the S-RIO data flows are vastly different. Similarly, the same architecture that would target different wireless standards, such as WCDMA vs. LTE, would require a different S-RIO data flow. For that reason, it would be wise to model the S-RIO traffic scenarios within the system to ensure the size and speed of each link is adequate to perform the necessary algorithm within the timing budget of each standard.

S-RIO offers link widths of 1x, 2x and 4x, and link speeds ranging from 1.25 to 6.25

Gb/s. Figure 1 and Figure 2 show S-RIO links of 4x, but some systems can be performed with smaller links where appropriate depending on the number of users serviced and the capabilities of each DSP involved.

#### Conclusion

Serial RapidIO is the only interconnect technology defined to address a distributed array of processors arranged in any topology with easy routing and adaptability. Its simplistic approach to routing packets based on the Destination ID field makes it easy for software implementers to discover new nodes in a system or redistribute traffic in the case of processor failures.

Serial RapidIO is scalable while maintaining the same software programming model without complications of memory map management common with other protocols. No other protocol can make the two architectures discussed above into “Software Programmable Base Stations.” For more information about the Serial RapidIO protocol, please visit www.rapidio.org and for more information about IDT Serial RapidIO switches and enablement tools, please visit http://www.IDT.com/go/SRIOSwitches.

Stephane Gagnon, director of product management, joined IDT in August 2000. For the past 10 years, Stephane has been involved in the RapidIO Trade Association Technical Working Group and currently holds the position of Chairman of the Trade Association Steering Committee.

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