Power Efficiency

The path to achieving energy efficiency is ridden with obstacles.

Q: If we continue to increase the power efficiency of a product, are we approaching the point of diminishing returns? Will it eventually detrimentally impact the cost of the product?

Doug Bailey, VP marketing, Power Integrations

This is an interesting question. Certainly regulatory bodies worldwide have embarked with enthusiasm on campaigns to encourage makers of a wide range of products to reduce power consumption. While there has been an inevitable 'push back' from a minority of affected parties and consumer groups, mostly industry has reacted very well and products now comply with a range of voluntary and mandatory standards, such as ENERGY STAR and the European Union's Ecodesign programs.

But whether this drive for ultimate efficiency can continue without forcing consumers to dig too deeply into their pockets is complex issue.

One area that has grabbed much attention is the move to reduce standby power (the amount of power consumed when an item, such as a charger or TV set, is inactive but still switched on at the mains). We find that improving standby performance is a matter of intelligent design and not system cost – since silicon complexity is very inexpensive – and so we're very enthusiastic about our ability to further reduce standby and no-load power losses.

However, active power consumption is another matter: Power conversion efficiency is given by the ratio of Output Power divided by Input Power and has a very significant impact on cost.

Designers can use ICs, such as Power Integrations' TopSwitch™-JX, to build power supplies based on the flyback topology which can achieve upwards of 90% efficiency, depending on the precise power supply specification. If it is essential

(dare I say, ‘mandated’) to achieve greater levels of efficiency, then designers may be forced to consider “two-switch” topologies such as LLC, two-switch-forward, or half-bridge. There are other options, such as adding an active clamp to recover leakage energy or using synchronous rectification – but any of these solutions has a substantial cost implication.

So we come back to trade-offs, and in most instances the pragmatic approach is to consider power levels. I don’t know how to make a 97%-efficient cell phone adapter using flyback converter technology, and other known topologies make the power supply more expensive. My conclusion is that for low-power products that don’t use much energy in the first place, a relatively inefficient, but optimized, solution based on an inexpensive topology is a good way to go. However, for higher power applications above 100 W, it is not only possible – but practical and affordable – to aim for higher efficiencies because the payback in energy saved does eventually cover the cost of the incremental hardware needed to achieve the efficiency gains.

Tom Sandoval, CEO, Calypto Design Systems

Achieving the most optimized solution for any particular design characteristic will always need to be balanced against the need to meet the market requirements for a product. The real challenge is the ability of the engineers designing the product to make those tradeoffs quickly and accurately. If they are not able to, realizing the most optimal product that achieves the right tradeoffs becomes difficult. Because of the complexity of today’s electronics systems and shrinking design cycles driven by consumer demand and increased global competition, the use of tools that automatically perform these tradeoffs can be a significant competitive advantage.

In the case of the power efficiency of the ICs that go into today’s electronics systems, evaluating design tradeoffs to achieve the lowest power dissipation possible has been a significant challenge. Today, most IC designers use a manual approach to achieving the lowest power design. The actual design changes are implemented manually through a trial and error process. That is, designers use their experience and intuition to make changes that they think will reduce design power. They then use a variety of time consuming, complex methods to verify that the silicon area (cost) and performance of the device have not been impacted and that the functionality of the design remains consistent with the original design. However, as the complexity of ICs continues to increase, the combination of this “hit or miss” power optimization approach combined with the amount of time required to

evaluate the performance/area impact is now delivering diminishing returns.

The solution is the use of a fully automated capability for power optimization across the entire IC that ensures power savings, but does not impact area and performance. Calypto's PowerPro product automatically reduces power across all of the elements of an IC including the logic, storage elements (registers and memories) and clock tree. PowerPro uses Calypto's patented sequential analysis technology to generate changes to a design that reduce power. PowerPro's internal prototyping engine then determines an optimal set of design changes to reduce power while ensuring that there is no impact to area or performance. In addition, Calypto's automated flow includes the use of SLEC Pro to formally verify that the power optimized design is functionally equivalent to the original design.

To answer the question more directly, in the case of ICs, the manual modification of designs for power reduction is approaching diminishing returns. However, products are available — PowerPro from Calypto — that provide new opportunities for power savings and do not impact the other key characteristics of the design.

Source URL (retrieved on *04/17/2014 - 4:03am*):
http://www.wirelessdesignmag.com/articles/2010/07/power-efficiency?qt-blogs=0