Next Generation PoP for Processor and Memory Stacking

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Figure 1

Assembly Package Size	10mm	12mm	14mm
Top # I/O	96	128	152
Bottom # I/O	300	400	550
Max Die Size (mm)	5.5	7.5	9.0
Package Thickness (mm)	1.4+		

[1]

The continued increase in mobile handset functionality is being enabled by more powerful baseband and applications processor chips, which are more frequently coupled with memory devices using package-on-package (PoP) stacking. These handset functions and processor capacities are increased through advances made in semiconductor fabrication process technology. For example, the baseband and applications processors are requiring more interconnects, forcing a conversion to area array flip chip packaging. However, the transition from wire bond to flip chip presents challenges and opportunities for PoP design and assembly.

PoP stacking is driven primarily by the need to reduce package footprint in mobile phones and other hand-held electronic devices. In addition to requiring less space on the motherboard than individual memory and logic packages placed side by side, a PoP stack provides better electrical performance by reducing the length of connections between the parts. PoP package layouts conform to the JEDEC Solid State Technology Association standards, allowing manufacturers to source logic and

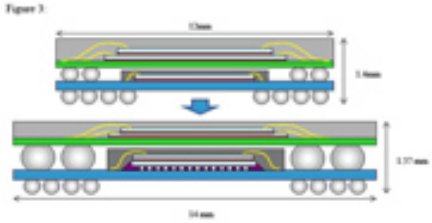
[2]

memory devices from different suppliers. The typical PoP memory on logic stack has a top to bottom BGA interconnect pitch of 0.65mm and a BGA pitch of 0.50mm from the bottom package to the motherboard. The maximum height of a typical PoP with 2 memory dies in the top package today is 1.3-1.4mm. However, it is usually taller as many PoP packages have more than 2 memory die stacked in the upper package (see Figure 1).

The market for smart phones is growing, with over 500M units expected to ship in 2013. Consumers are expecting all-in-one functionality, including mobile Internet, video, GPS, camera and games. The demand for increased performance is causing

the processor chip size to grow and require more interconnects. Meanwhile, package form factors are expected to remain the same or even shrink to fit into smaller and slimmer devices.

Flip Chip Bottom Package Provides Flexibility



[3]

The use of flip chip interconnect technology in the bottom package provides more flexibility for the PoP stack. Replacing the die level interconnect with flip chip increases the X/Y space available for either an increased number of top-to-bottom connections or for a larger processor chip. A flip chip die is underfilled and therefore does not need to be overmolded. This reduces the X/Y area required as keep out areas for wire bonds are not needed. Eliminating the overmold reduces the gap height between the top and bottom packages allowing the use of smaller solder balls on a tighter interconnect pitch (see Figure 2).

Alternatively, an increase in functionality can be achieved by using a flip chip die on the lower package and stacking of a second die on top of the flip chip. This second die would require wire bond interconnects and overmold which drives the PoP interconnects to increased height requiring larger solder balls and hence larger pitch. Stacking a second chip on the bottom may also require more connections to the top package. The overall package would have to grow taller and wider to accommodate this, or a high aspect ratio fine pitch solution for top to bottom package interconnect would have to be used (Figure 3).

Stacked Die in Bottom Package Requires PoP Interconnect Innovation

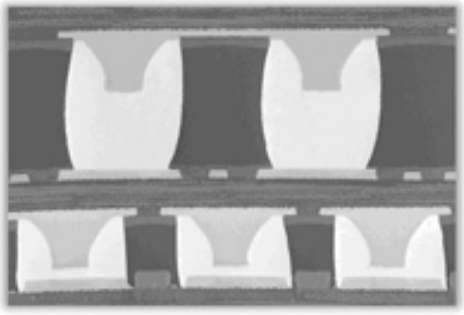


Figure 4: The pPILR provides tall columnar solder connections at fine pitch for large top-to-bottom standoff heights and low profile bottom package mounting to the motherboard.

[4]

As processors become more powerful, and functionality increases, even a single die in the bottom package can require more connections to the top package than what is available with the current lowest standard top-to-bottom pitch of 0.5mm (ex: 168

I/O for a 12mm package). Increasing the package footprint to fit more top package to bottom package interconnects, or adding more rows within the current footprint and reducing die size, is generally not feasible, therefore a fine pitch solution would have to be used.

One solution to increasing package density while keeping or reducing the package footprint is Tessera's µPILR PoP (see Figure 4).

The small high aspect ratio pillars elevate the wetting surface for solder interconnect above the surface of the substrate effectively reaching toward a smaller solder ball that can be placed at finer pitch. Once wetted to the µPILR, the solder will wick into solder columns maintaining adequate separation to avoid solder bridging between the vertical interconnects. This enables PoP stacking at fine pitch with standoff heights effectively increased by the height of the µPILR. This additional height margin provides flexibility for bottom package stacked die without increasing overall footprint saving package cost as well as motherboard area.

Figure 5: The µPILR Flip Chip posts provide increased margin for bump wetting at fine pitch and positive stand-off for underfilling.

[5]

Also, the elevated wetting surface provided by the highly planar pillars delivers higher stacking yield by providing margin to mitigate the open and shorted solder joints that result from substrate warping. In side-by-side stacking tests with substrates with typical warp, the µPILR interconnect showed no opens or shorts while the solder ball control parts showed many.

The µPILR PoP solution overcomes the limitations of conventional BGA technology, enabling manufacturers to deliver devices with lower profile, finer pitch and higher performance. µPILR enables pitch as low as 0.3mm while maintaining a standoff height of 0.2mm, resulting in a total package thickness of less than 1.0mm. This technology has the added benefit of high reliability because the µPILR interconnects have high fracture toughness under both static and dynamic loading. Finally, µPILR PoP uses standard materials and processes for assembly, requiring no new infrastructure investment.

Flip Chip Assembly with Thin Die and Thin Package Substrate is a Challenge

In addition to PoP, µPILR technology could be used for the bottom flip chip package, attaching the flip chip die to the package via copper pillars on substrate instead of copper posts on die (see Figure 5).

µPILR provides a highly coplanar bump interconnect layer with increased wetting margin for bump joining. This is very important for maintaining high yields when assembling large thin devices with

Figure 6:

	JEDEC BGA PoP		Tessera uPILR FC PoP	
Package Size	12	12	12	12
Total Thickness	1.4	1.4	1.0	1.0
Pitch at Top (mm)	0.65	0.5	0.4	0.3
# I/O at Top	128	168	216	296
Maximum Die size	8.40	8.75	8.95	9.2

[6]

higher bump count to very thin package substrates prone to warpage. µPILR interconnect for flip chip also enables higher I/O (input / output) devices by scaling down to <100µm pitch. It enables predictable stand-off heights for high underfill yields even with collapsible lead-free solder bumps and reduces the risk of electromigration damage because the reduced pitch does not necessarily require a die pad size reduction and the resulting current crowding (see Figure 6).

Consumer demand continues to grow for slimmer and more powerful, feature rich, all-in-one handheld electronics. To satisfy the demand, PoP devices must continue shrinking while increasing interconnect density for greater processing power. Using flip chip for the bottom package die helps reduce package size, but using conventional solder balls limits progress. The µPILR interconnect solution for both the PoP and Flip Chip interconnects enables further integration of functionality and continued miniaturization of electronic devices.

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