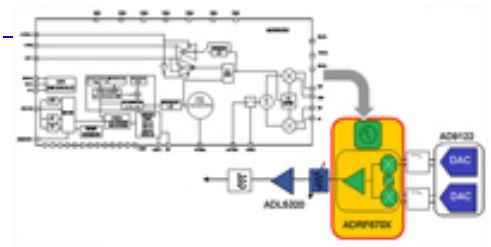
Transmitter RFIC Integration for Next Generation Wireless Infrastructure Radios

Leveraging highly integrated RFIC designs and high dynamic range converters helps meet the challenges of next-generation base stations.

By Phillip Halford and Ed Balboni, RF Group, Analog Devices, Inc.

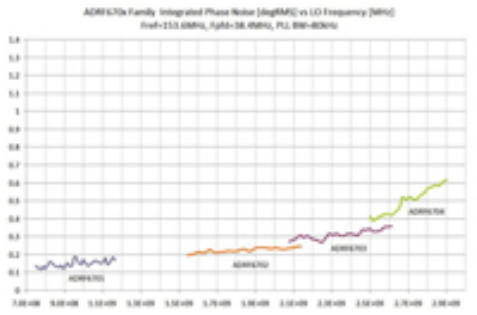


[1]

The migration to 3G and LTE Advance for the next generation of mobile communications infrastructure equipment provides many challenges for the equipment and component suppliers. Next generation radios are required to support wider signal bandwidths with more complex modulations for greater data rates across a broader number of operating frequency bands for world wide deployment. The performance in terms of noise, signal linearity, power consumption and physical size are all critical and more demanding as component suppliers are also expected to reduce cost and space for higher density applications.

This provides increased challenges for the RFIC designer as integration needs to equal or better the performance of discrete implementation. With a discrete implementation, the system designer can pick and use devices optimized and designed for optimum performance using different technologies such as GaAs, Si Bipolar or CMOS. But this flexibility to select optimum process technology provides the greatest challenge for RFIC designer looking to offer higher levels of integration within a single process technology.

Within the base station transmitter, the analog I/Q modulator is the key RFIC component in determining the noise floor and linearity of the transmit signal path, so any relaxation in performance to reduce the size, power or cost is unacceptable.



[2]

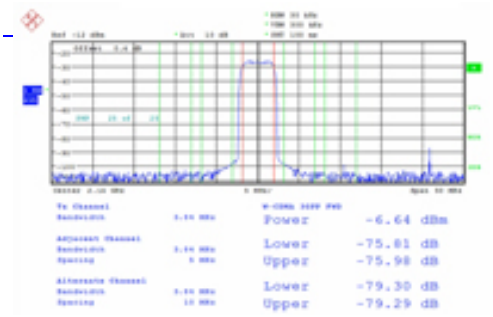
Fortunately SiGe BiCMOS process technology is uniquely suited toward higher levels of integration without sacrificing performance. These processes typically offer multiple speed-breakdown SiGe NPN transistors and in some cases complementary high-performance PNP transistors coupled with one, or more frequently two, CMOS transistor feature sizes. To this base is added an array on MIM capacitors, thin-film resistors and importantly multiple thick copper and aluminum metallization. These features allow the designer to implement multiple high performance functional blocks on a single IC thus realizing substantial power and size savings while maintaining very high levels of performance.

Base Station LO Distribution

One of the important aspects of transmitter board level design is the local oscillator synthesis and distribution for the various up and down frequency conversion stages. The basestation LO distribution must retain phase coherence to all distant corners of the PCB and must also have low in-band and low wideband noise and low overall spurious content. The mixer performance is only be as good as the LO driving it, so a high quality LO is a critical element in the overall transmitter performance. In addition, very small amounts of phase noise, or spurious components on LO signals, can induce enough energy into analog signal paths to cause the transmitter to fail spurious emissions set by the major cellular communications standards (MC-GSM, WCDMA, LTE, WiMAX). The required LO for these standards ranges from about 500MHz to near 4GHz, which means that layout for the LO distribution must be handled with great care. The length of the traces from LO generation to its final termination should be kept as short as possible, but this is often difficult if the LO synthesizer must feed several different devices. One solution is to feed a common low frequency reference to a separate PLL synthesizers near each required LO, but this takes up significant real estate on the PCB.

The ADRF670x family of integrated modulators solves many of these problems, through the integration with a state of the art fractional-N PLL, and an integrated VCO. Using silicon germanium technology allows industry leading dynamic range in both the quadrature modulator and mixer with VCO to achieve performance that is competitive and significantly smaller than external VCO/PLL solutions. The VCO is implemented in upper level thick metal layers to build high Q on chip inductors as part of the LC tank. The VCO capacitor is formed using MOS switchable MIM capacitors allowing the VCO to switch frequencies over a wide frequency range with low phase noise. The band is automatically adjusted each time the PLL frequency is programmed thus providing a self-contained and reliable solution. The band size is

chosen to ensure operation over the full temperature range once initially set. Thick metal is also used to integrate an output balun with excellent return loss for during subsequent stages. The ADRF670x family consists of 4 overlapping family members to cover frequency range and bands from 400MHz to 3GHz. Each family member is specified based on the output balun bandwidth over a 1dB and 3dB pass band.



[3]

The ADRF670x and ADRF660X families fractional-N PLL design is ideally suited for low phase noise 3G and 4G applications. These new cellular standards, with their densely spaced signal constellations, require increasingly lower LO integrated phase noise to maintain full performance. Traditional PLL synthesizer design uses an "Integer-N" architecture, where the output frequency is an integer multiple of the phase-detector frequency. In order to provide small step sizes in frequency, the integer multiplication factor must be very large. A significant amount of the LO phase noise originates in the reference path and is amplified by the PLL frequency multiplication factor. This results in high in-band noise at the PLL output. A fractional-N PLL allows small step sizes in output frequency, while keeping the overall frequency multiplication low, therefore reducing phase noise amplification compared with integer-N PLLs.

Adjacent Channel Power Ratio Measurement

Adjacent Channel Power Ratio (ACPR) is a measurement which determines how much of a transmitted signal leaks into adjacent frequency bands. 3G standards such as WCDMA are very strict on the amount of power allowed to be transmitted out of band. The ACPR measurement for the ADRF6702 is shown in figure 3. The modulator provides highly linear output power and low noise enabling better than -76dB ACPR at -6dBm output. This helps reduce the number of gain stages following the modulator and maximize the dynamic range prior to the final power amplifier stages.

The ADRF670X family further simplifies user application, cost and board area through the integration of 3 LDO circuits enabling operation off a single 5V supply. The LDOs are used to supply a regulated supply to the VCO, the charge pump, and PLL sigma delta modulator, while the +5V supply is used directly with e I-Q modulator to maximize the output power.

In high density applications one ADL670X can synthesize an LO internally using its PLL, while other the other devices can disable their PLLs and use the common LO from the one master device.

The ADRF670X family as shown in figure 4 has been designed to minimize and ease the user interface to ADI's latest transmit digital to analog converter AD9122 and GaAs amplifiers such as the ADL5320 a ¼ watt high linearity amplifier capable of driving >0dBm into the final PA stage. This combination of devices completes the active IC content in three compact IC and is suitable for all cellular next generation multicarrier radio platforms.

Conclusion

Multicarrier 3G and LTE 4G base stations will deliver a dramatic increase in data rates than what exists today. The migration to these next generation standards poses a number of challenges for base station manufacturers as they are under pressure to increase performance, capacity and density, while reducing the size of the base station and bill of materials cost. In order to address these challenges, increased pressure is then placed upon integrated circuit manufacturers, specifically within the radio signal path, to deliver very high performance components that are capable of addressing a wide dynamic range and that, without sacrificing performance, integrate multiple functions in order to reduce the footprint and thereby BOM costs. By leveraging highly integrated RFIC designs and high dynamic range converters, designers can effectively reduces the component count of next generation base stations by 60 percent.

By Phillip Halford is product marketing manager, RF Group, Analog Devices, Inc. He can be reached at phillip.halford@analog.com. Ed Balboni is a design engineer, RF Group, Analog Devices, Inc. Balboni can be reached at ed.balboni@analog.com.

Links:
[1] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/1002/ADI_TechFea1_lrg.jpg
[2] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/1002/ADI_TechFea2_lrg.jpg
[3] http://www.wirelessdesignmag.com/sites/wirelessdesignmag.com/files/legacyimages/1002/ADI_TechFea3_lrg.jpg